

UMA & Optimus Schematics Document

IVY Bridge(rPGA989)

Intel PCH(Panther Point)

DY :NotInstalled

UMA:UMA platform installed

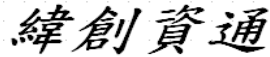
OPS:Optimus

HR:Huron River

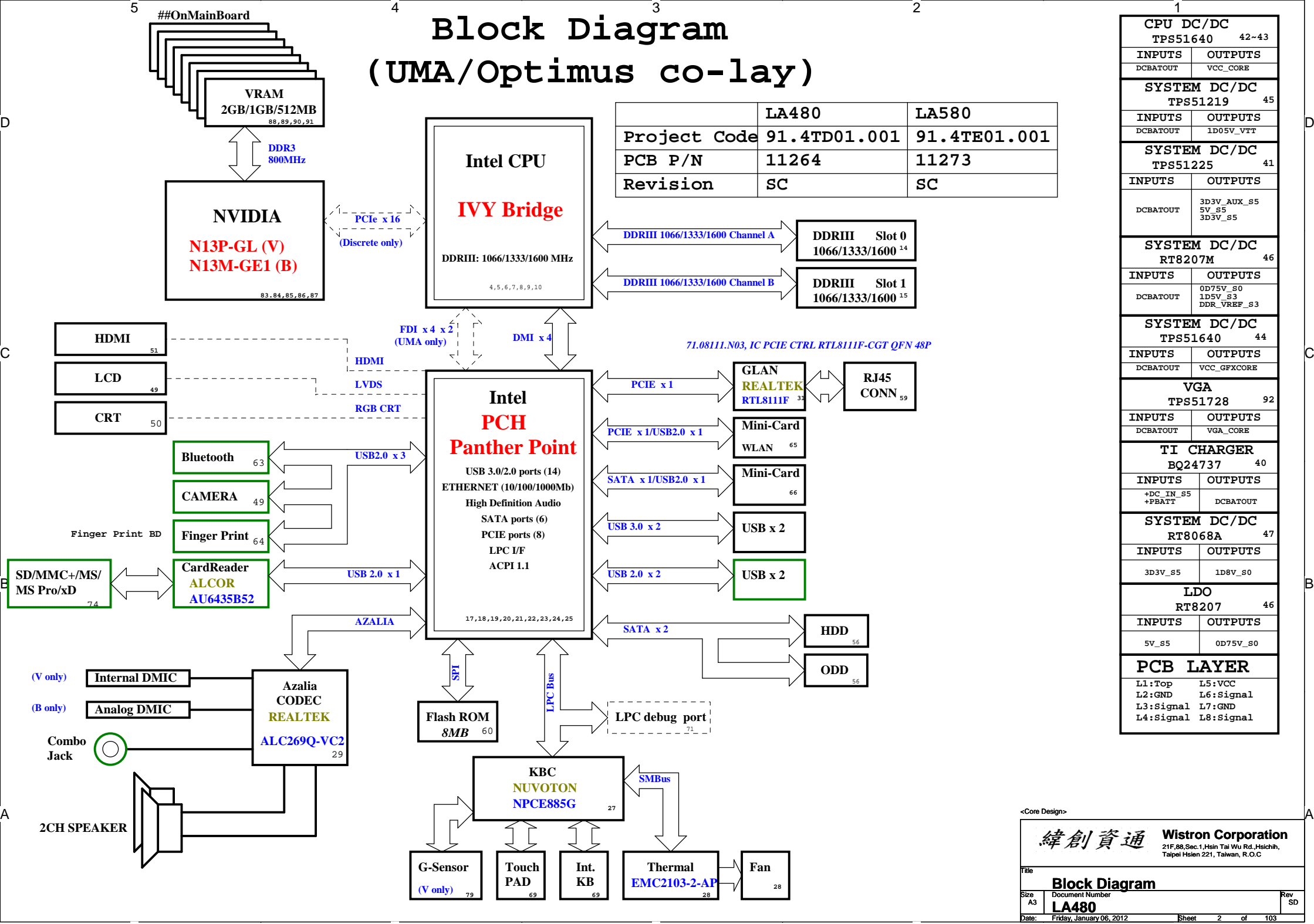
CR:Chief River

V: V-Series installed

<Core Design>

		Wistron Corporation 21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C	
Title			
Cover Page			
Size A4	Document Number LA480		Rev SD
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Block Diagram (UMA/Optimus co-lay)



PCH Strapping Chief River Schematic Checklist Rev0.72

Name	Schematics Notes
SPKR	Reboot option at power-up Default Mode: Internal weak Pull-down. No Reboot Mode with TCO Disabled: Connect to Vcc3_3 with 8.2-kΩ - 10-kΩ weak pull-up resistor.
INIT3_3V#	Weak internal pull-up. Leave as "No Connect".
GNT3#/GPIO55 GNT2#/GPIO53 GNT1#/GPIO51	GNT[3:0]# functionality is not available on Mobile. Mobile: Used as GPIO only Pull-up resistors are not required on these signals. If pull-ups are used, they should be tied to the Vcc3_3power rail.
SPI_MOSI	Enable Danbury: Connect to Vcc3_3 with 8.2-k? weak pull-up resistor. Disable Danbury: Left floating, no pull-down required.
NV_ALE	Enable Danbury: Connect to +NVRAM_VCCQ with 8.2-kohm weak pull-up resistor [CRB has it pulled up with 1-kohm no-stuff resistor] Disable Danbury: Leave floating (internal pull-down)
NC_CLE	DMI termination voltage. Weak internal pull-up. Do not pull low.
HAD_DOCK_EN# /GPIO[33]	Low (0) - Flash Descriptor Security will be overridden. Also, when this signals is sampled on the rising edge of PWROK then it will also disable Intel ME and its features. High (1) - Security measure defined in the Flash Descriptor will be enabled. Platform design should provide appropriate pull-up or pull-down depending on the desired settings. If a jumper option is used to tie this signal to GND as required by the functional strap, the signal should be pulled low through a weak pull-down in order to avoid asserting HDA_DOCK_EN# inadvertently. Note: CRB recommends 1-kohm pull-down for FD Override. There is an internal pull-up of 20 kohm for DA_DOCK_EN# which is only enabled at boot/reset for strapping functions.
HDA_SDO	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
HDA_SYNC	Weak internal pull-down. Do not pull high. Sampled at rising edge of RSMRST#.
GPIO15	Low(0) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with no confidentiality. High(1) - Intel ME Crypto Transport Layer Security (TLS) cipher suite with confidentiality. Note : This is an un-muxed signal. This signal has a weak internal pull-down of 20 kohm which is enabled when PWROK is low. Sampled at rising edge of RSMRST#. CRB has a 1-kohm pull-up on this signal to +3.3VA rail.
GPIO8	GPIO8 on PCH is the Integrated Clock Enable strap and is required to be pulled-down using a 1k +/- 5% resistor. When this signal is sampled high at the rising edge of RSMRST#, Integrated Clocking is enabled, When sampled low, Buffer Through Mode is enabled.
GPIO27	Default = Do not connect (floating) High(1) = Enables the internal VccVRM to have a clean supply for analog rails. No need to use on-board filter circuit. Low (0) = Disables the VccVRM. Need to use on-board filter circuits for analog rails.

PCIe Routing

LANE1	X
LANE2	Mini Card2(WWAN)
LANE3	Card Reader
LANE4	Mini Card1(WLAN)
LANE5	X
LANE6	Intel GBE LAN / LAN
LANE7	X
LANE8	Express Card

USB Table port9 is debug port

Pair	Device
0	USB3.0 ext port 1
1	USB3.0 ext port 2
2	USB3.0 ext port 3
3	USB3.0 ext port 4
4	BLUETOOTH (USB1.1)
5	Fingerprint (USB1.1)
6	X
7	X
8	Mini Card2 (WWAN)
9	USB ext. port 4 / E-SATA /USB CHARGER
10	CARD READER
11	Mini Card1 (WLAN)
12	CCD
13	New Card

Processor Strapping Chief River Schematic Checklist Rev0.72

Pin Name	Strap Description	Configuration (Default value for each bit is 1 unless specified otherwise)	Default Value
CFG[2]	PCI-Express Static Lane Reversal	1: Normal Operation. 0: Lane Numbers Reversed 15 -> 0, 14 -> 1, ...	1
CFG[4]		Disabled - No Physical Display Port attached to Embedded DisplayPort. 1: Embedded DisplayPort. 0: Enabled - An external Display Port device is connectd to the EMBEDDED display Port	0
CFG[6:5]	PCI-Express Port Bifurcation Straps	11 : x16 - Device 1 functions 1 and 2 disabled 10 : x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01 : Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00 : x8, x4, x4 - Device 1 functions 1 and 2 enabled	11
CFG[7]	PEG DEFER TRAINING	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training	1

POWER PLANE	VOLTAGE	Voltage Rails	DESCRIPTION
		ACTIVE IN	
5V_S0 3D3V_S0 1D8V_S0 1D5V_S0 1D05V_VTT 1D0V_S0 VCCSA UD75V_S0 VCC_CORE VCC_GFXCORE 1D8V_VGA_S0 3D3V_VGA_S0 1V_VGA_S0	5V 3.3V 1.8V 1.5V 1.05V 1.0V 0.9 - 0.675V 0.75V 0.35V to 1.5V 0.4 to 1.25V 1.8V 3.3V 1V	S0	CPU Core Rail Graphics Core Rail
5V_USBX_S3 1D5V_S3 DDR_VREF_S3	5V 1.5V 0.75V	S3	
BT+ DCBATOUT 5V_S5 5V_AUX_S5 3D3V_S5 3D3V_AUX_S5	6V-14.1V 6V-14.1V 5V 5V 3.3V 3.3V	All S states	AC Brick Mode only
1D05V_LAN	1.05V	S0/M0, SX/M3	ON whenever iAMT is active
3D3V_M 1D05V_M	3.3V 1.05V	S0/M0, SX/M3, WOL_EN	ON for iAMTLegacy WOL
3D3V_AUX_KBC	3.3V	DSW, Sx	ON for supporting Deep Sleep states
3D3V_AUX_S5	3.3V	G3, Sx	Powered by Li Coin Cell in G3 and 3D3V_S5 in Sx

SATA Table

SATA	
Pair	Device
0	HDD1
1	mSATA
2	N/A
3	N/A
4	ODD
5	ESATA

SMBus ADDRESSES

I 2 C / SMBus Addresses	Ref Des	Chief River CRV
Device	Address	Hex Bus
EC SMBus 1 Battery CHARGER		BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA BAT_SCL/BAT_SDA
EC SMBus 2 PCH eDP		SMML1_CLK/SMML1_DATA SMML1_CLK/SMML1_DATA SMML1_CLK/SMML1_DATA
PCH SMBus SO-DIMMA (SPD) SO-DIMMB (SPD) Digital Pot G-Sensor MINI		PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK PCH_SMBDATA/PCH_SMBCLK

<Core Design>

緯創資通

Wistron Corporation

21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.

Title

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Size A3

Document Number

Rev SD

Date: Friday, January 06, 2012

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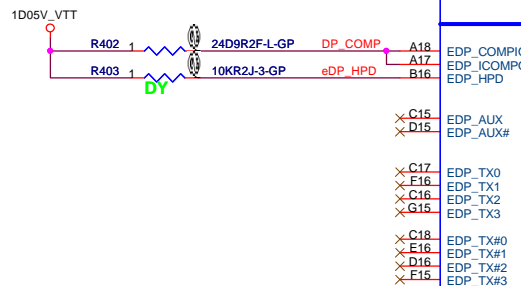
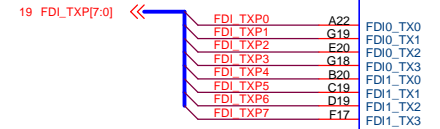
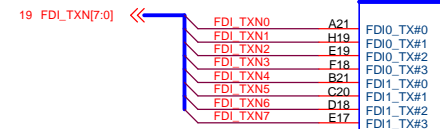
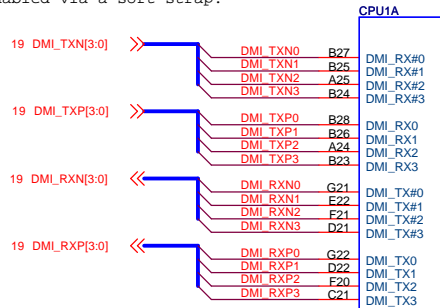
SSID = CPU

01.00IVY.000 IVY BRIDGE ORCAD SYMBOL.

Note:
Intel DMI supports both Lane
Reversal and polarity inversion
but only at PCH side. This is
enabled via a soft strap.

Signal Routing Guideline:
PEG_ICOMPO keep W/S=12/15 mils and routing length less than 500 mils.
PEG_ICOMPI & PEG_RCOMPO keep W/S=4/15 mils and routing length less than 500 mils.

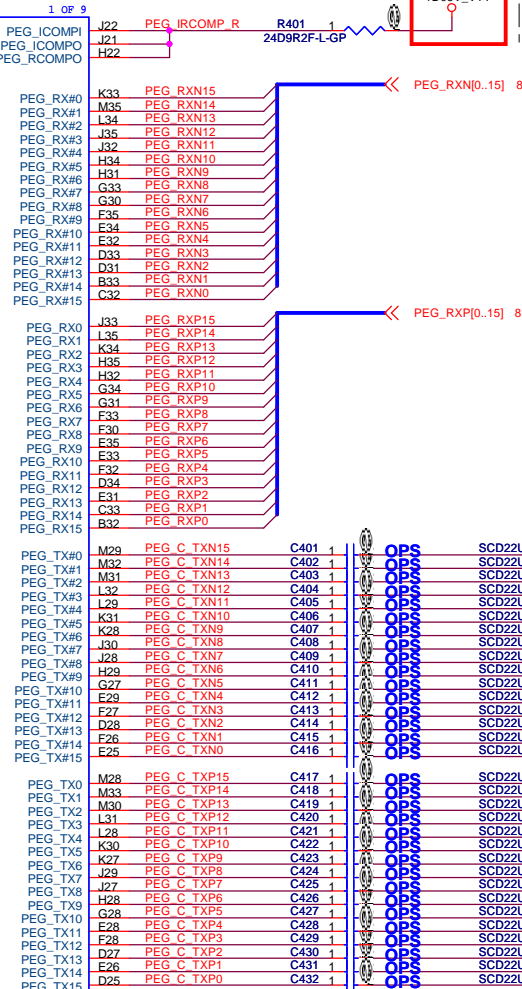
NOTE:
If PEG is not implemented, the RX&TX pairs can be left as No Connect



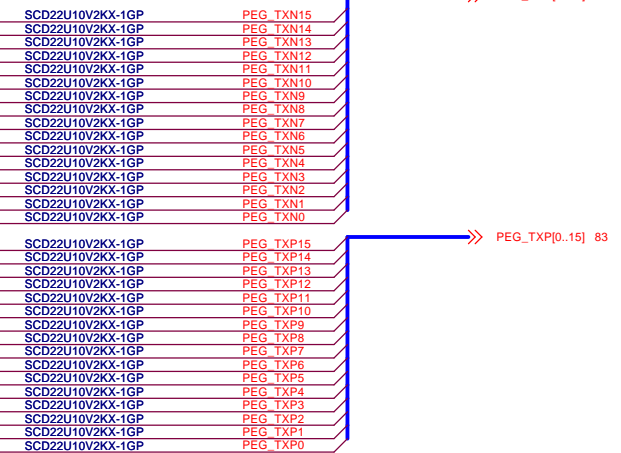
SANDY
62.10055.421
2nd = 62.10040.771

SKT-BGA989C470395-1H180

DMI
Intel(R) FDI
PCI EXPRESS* - GRAPHICS



PEG Static Lane Reversal



Note:
Intel FDI supports both Lane
Reversal and polarity inversion
but only at PCH side. This is
enabled via a soft strap.

Note:
Lane reversal does not apply to
FDI sideband signals.

NOTE:
Select a Fast FET similar to 2N7002E whose rise/
fall time is less than 6 ns. If HPD on eDP interface is
disabled, connect it to CPU VCCIO via a 10-kΩ pull-Up
resistor on the motherboard.

Signal Routing Guideline:
EDP_ICOMPO keep W/S=12/15 mils and routing
length less than 500 mils.
EDP_COMPIO keep W/S=4/15 mils and routing
length less than 500 mils.

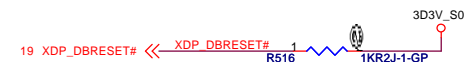
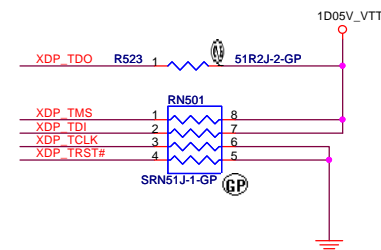
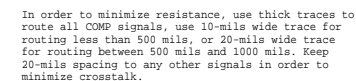
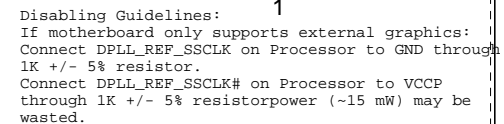
NOTE:
Processor strap CFG[4] should be pulled low to enable Embedded DisplayPort.

<Core Design>

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DEL U501
DEL R519
DEL C503
DEL R517
DEL R515

ASM R510
ASM R509



SSID = CPU

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SANDY

DDR SYSTEM MEMORY A

M A DQ0 C5 SA DQ0
M A DQ1 D5 SA DQ1
M A DQ2 D3 SA DQ2
M A DQ3 D2 SA DQ3
M A DQ4 D6 SA DQ4
M A DQ5 C6 SA DQ5
M A DQ6 C2 SA DQ6
M A DQ7 C3 SA DQ7
M A DQ8 F10 SA DQ8
M A DQ9 F8 SA DQ9
M A DQ10 G10 SA DQ10
M A DQ11 G9 SA DQ11
M A DQ12 F9 SA DQ12
M A DQ13 F7 SA DQ13
M A DQ14 G8 SA DQ14
M A DQ15 G7 SA DQ15
M A DQ16 K4 SA DQ16
M A DQ17 K5 SA DQ17
M A DQ18 K1 SA DQ18
M A DQ19 J1 SA DQ19
M A DQ20 J5 SA DQ20
M A DQ21 J4 SA DQ21
M A DQ22 J2 SA DQ22
M A DQ23 K2 SA DQ23
M A DQ24 M8 SA DQ24
M A DQ25 N10 SA DQ25
M A DQ26 N8 SA DQ26
M A DQ27 N7 SA DQ27
M A DQ28 M10 SA DQ28
M A DQ29 M9 SA DQ29
M A DQ30 M7 SA DQ30
M A DQ31 AG6 SA DQ31
M A DQ32 AG6 SA DQ32
M A DQ33 AG5 SA DQ33
M A DQ34 AG5 SA DQ34
M A DQ35 AG5 SA DQ35
M A DQ36 AH6 SA DQ36
M A DQ37 AH6 SA DQ37
M A DQ38 AJ5 SA DQ38
M A DQ39 AJ6 SA DQ39
M A DQ40 AJ8 SA DQ40
M A DQ41 AJ8 SA DQ41
M A DQ42 AJ9 SA DQ42
M A DQ43 AK9 SA DQ43
M A DQ44 AH8 SA DQ44
M A DQ45 AH9 SA DQ45
M A DQ46 AL9 SA DQ46
M A DQ47 AL8 SA DQ47
M A DQ48 AP11 SA DQ48
M A DQ49 AN11 SA DQ49
M A DQ50 AL12 SA DQ50
M A DQ51 AM12 SA DQ51
M A DQ52 AM11 SA DQ52
M A DQ53 AL11 SA DQ53
M A DQ54 AP12 SA DQ54
M A DQ55 AN12 SA DQ55
M A DQ56 AJ14 SA DQ56
M A DQ57 AH14 SA DQ57
M A DQ58 AL15 SA DQ58
M A DQ59 AK15 SA DQ59
M A DQ60 AL14 SA DQ60
M A DQ61 AK14 SA DQ61
M A DQ62 AJ15 SA DQ62
M A DQ63 AH15 SA DQ63

SA_CLK0 AB6 M A DIM0_CLK_DDR0 14
SA_CLK#0 AA6 M A_DIM0_CLK_DDR#0 14
SA_CKE0 V9 M A_DIM0_CKE0 14

SA_CLK1 AA5 M A_DIM0_CLK_DDR1 14
SA_CLK#1 AB5 M A_DIM0_CLK_DDR#1 14
SA_CKE1 V10 M A_DIM0_CKE1 14

SA_CLK2 AB4
SA_CLK#2 AA4
SA_CKE2 W9

SA_CLK3 AB3
SA_CLK#3 AA3
SA_CKE3 W10

SA_CS#0 AK3 M A_DIM0_CS#0 14
SA_CS#1 AL3 M A_DIM0_CS#1 14
SA_CS#2 AG1
SA_CS#3 AH1

SA_ODT0 AH3 M A_DIM0_ODT0 14
SA_ODT1 AG3 M A_DIM0_ODT1 14
SA_ODT2 AG2
SA_ODT3 AH2

SA_DQS#0 C4 M A DQS#0 M A_DQS#7:0 14
SA_DQS#1 G6 M A DQS#1
SA_DQS#2 J3 M A DQS#2
SA_DQS#3 M6 M A DQS#3
SA_DQS#4 AL6 M A DQS#4
SA_DQS#5 AM8 M A DQS#5
SA_DQS#6 AR12 M A DQS#6
SA_DQS#7 AM15 M A DQS#7

SA_DQS0 D4 M A DQS0 M A_DQS7:0 14
SA_DQS1 F6 M A DQS1
SA_DQS2 K3 M A DQS2
SA_DQS3 N6 M A DQS3
SA_DQS4 AL5 M A DQS4
SA_DQS5 AM9 M A DQS5
SA_DQS6 AR11 M A DQS6
SA_DQS7 AM14 M A DQS7

SA_MA0 AD10 M A A0 M A_A15:0 14
SA_MA1 W1 M A A1
SA_MA2 W2 M A A2
SA_MA3 W7 M A A3
SA_MA4 V3 M A A4
SA_MA5 V2 M A A5
SA_MA6 W3 M A A6
SA_MA7 W6 M A A7
SA_MA8 V1 M A A8
SA_MA9 W5 M A A9
SA_MA10 AD8 M A A10
SA_MA11 V4 M A A11
SA_MA12 W4 M A A12
SA_MA13 AF8 M A A13
SA_MA14 V5 M A A14
SA_MA15 V7 M A A15

SANDY
62.10055.421
2nd = 62.10040.771

CPU1D 4 OF 9

SANDY

DDR SYSTEM MEMORY B

M B DQ0 C9 SB DQ0
M B DQ1 A7 SB DQ1
M B DQ2 D10 SB DQ2
M B DQ3 C8 SB DQ3
M B DQ4 A9 SB DQ4
M B DQ5 A8 SB DQ5
M B DQ6 D9 SB DQ6
M B DQ7 D8 SB DQ7
M B DQ8 G4 SB DQ8
M B DQ9 F4 SB DQ9
M B DQ10 F1 SB DQ10
M B DQ11 G1 SB DQ11
M B DQ12 G5 SB DQ12
M B DQ13 F5 SB DQ13
M B DQ14 F2 SB DQ14
M B DQ15 J7 SB DQ15
M B DQ16 J7 SB DQ16
M B DQ17 J6 SB DQ17
M B DQ18 K10 SB DQ18
M B DQ19 K9 SB DQ19
M B DQ20 J8 SB DQ20
M B DQ21 J10 SB DQ21
M B DQ22 K6 SB DQ22
M B DQ23 K7 SB DQ23
M B DQ24 M5 SB DQ24
M B DQ25 N4 SB DQ25
M B DQ26 N2 SB DQ26
M B DQ27 N1 SB DQ27
M B DQ28 M4 SB DQ28
M B DQ29 M2 SB DQ29
M B DQ30 M1 SB DQ30
M B DQ31 M1 SB DQ31
M B DQ32 AM5 SB DQ32
M B DQ33 AM6 SB DQ33
M B DQ34 AR3 SB DQ34
M B DQ35 AP3 SB DQ35
M B DQ36 AN3 SB DQ36
M B DQ37 AN2 SB DQ37
M B DQ38 AN1 SB DQ38
M B DQ39 AP2 SB DQ39
M B DQ40 AP5 SB DQ40
M B DQ41 AN9 SB DQ41
M B DQ42 AT5 SB DQ42
M B DQ43 AT6 SB DQ43
M B DQ44 AP6 SB DQ44
M B DQ45 AN8 SB DQ45
M B DQ46 AR6 SB DQ46
M B DQ47 AR5 SB DQ47
M B DQ48 AR9 SB DQ48
M B DQ49 AJ11 SB DQ49
M B DQ50 AT8 SB DQ50
M B DQ51 AT9 SB DQ51
M B DQ52 AH11 SB DQ52
M B DQ53 AR8 SB DQ53
M B DQ54 AJ12 SB DQ54
M B DQ55 AH12 SB DQ55
M B DQ56 AT11 SB DQ56
M B DQ57 AN14 SB DQ57
M B DQ58 AR14 SB DQ58
M B DQ59 AT14 SB DQ59
M B DQ60 AT12 SB DQ60
M B DQ61 AR15 SB DQ61
M B DQ62 AR15 SB DQ62
M B DQ63 AT15 SB DQ63

SB_CLK0 AE2 M B DIM0_CLK_DDR0 15
SB_CLK#0 AD2 M B_DIM0_CLK_DDR#0 15
SB_CKE0 R9 M B_DIM0_CKE0 15

SB_CLK1 AE1 M B_DIM0_CLK_DDR1 15
SB_CLK#1 AD1 M B_DIM0_CLK_DDR#1 15
SB_CKE1 R10 M B_DIM0_CKE1 15

SB_CLK2 AB2
SB_CLK#2 AA2
SB_CKE2 T9

SB_CLK3 AA1
SB_CLK#3 AB1
SB_CKE3 T10

SB_CS#0 AD3 M B_DIM0_CS#0 15
SB_CS#1 AE3 M B_DIM0_CS#1 15
SB_CS#2 AD6
SB_CS#3 AE6

SB_ODT0 AE4 M B_DIM0_ODT0 15
SB_ODT1 AD4 M B_DIM0_ODT1 15
SB_ODT2 AD5
SB_ODT3 AE5

SB_DQS#0 D7 M B DQS#0 M B_DQS#7:0 15
SB_DQS#1 F3 M B DQS#1
SB_DQS#2 K6 M B DQS#2
SB_DQS#3 N3 M B DQS#3
SB_DQS#4 AN5 M B DQS#4
SB_DQS#5 AP9 M B DQS#5
SB_DQS#6 AK12 M B DQS#6
SB_DQS#7 AP15 M B DQS#7

SB_DQS0 C7 M B DQS0 M B_DQS7:0 15
SB_DQS1 G3 M B DQS1
SB_DQS2 J6 M B DQS2
SB_DQS3 M3 M B DQS3
SB_DQS4 AN6 M B DQS4
SB_DQS5 AP8 M B DQS5
SB_DQS6 AK11 M B DQS6
SB_DQS7 AP14 M B DQS7

SB_MA0 AA8 M B A0 M B_A15:0 15
SB_MA1 T7 M B A1
SB_MA2 R7 M B A2
SB_MA3 T6 M B A3
SB_MA4 T2 M B A4
SB_MA5 T4 M B A5
SB_MA6 T3 M B A6
SB_MA7 R2 M B A7
SB_MA8 T5 M B A8
SB_MA9 R3 M B A9
SB_MA10 AB7 M B A10
SB_MA11 R1 M B A11
SB_MA12 T1 M B A12
SB_MA13 AB10 M B A13
SB_MA14 R5 M B A14
SB_MA15 R4 M B A15

SANDY
62.10055.421
2nd = 62.10040.771

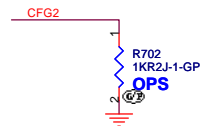
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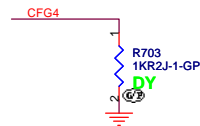
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Size			Document Number	Rev
A3			LA480	SD
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SSID = CPU



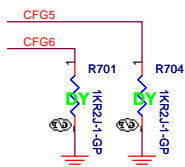
PEG Static Lane Reversal - CFG2 is for the 16x

CFG2	1: Normal Operation; Lane # definition matches socket pin map definition 0: Lane Reversed
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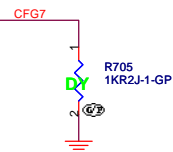
Display Port Presence Strap

CFG4	1: Disabled; No Physical Display Port attached to Embedded Display Port 0: Enabled; An external Display Port device is connected to the Embedded Display Port
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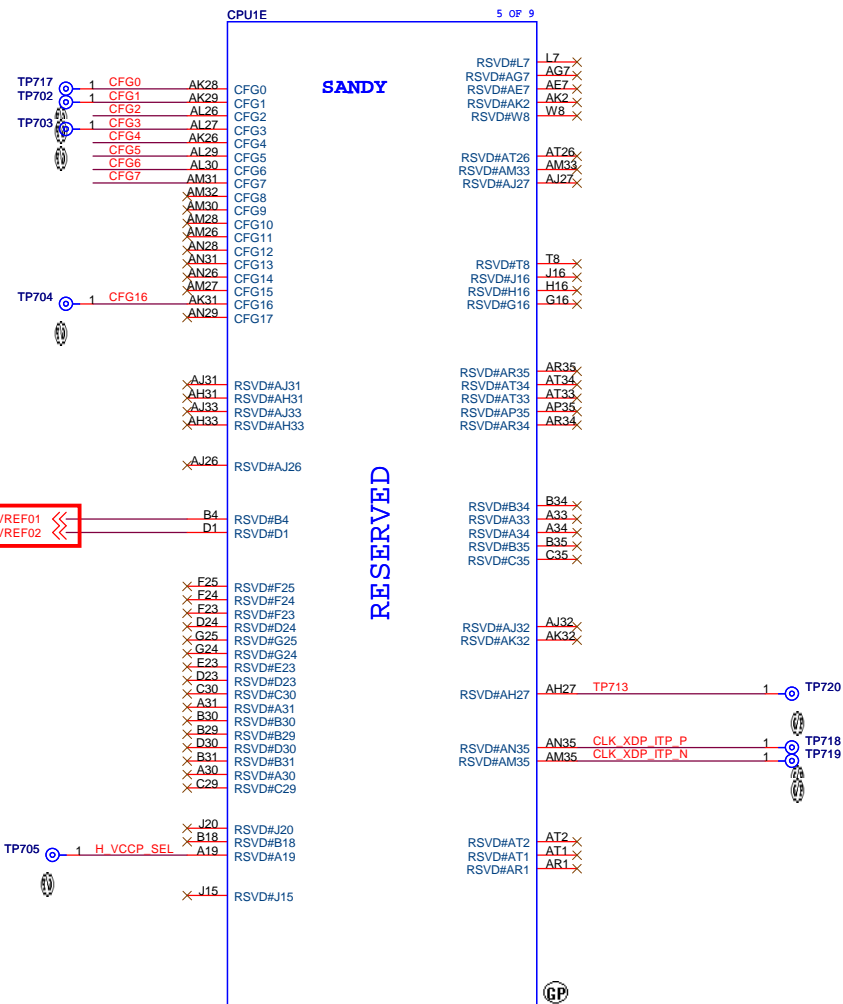
PCIe Port Bifurcation Straps

CFG[6:5]	11: x16 - Device 1 functions 1 and 2 disabled 10: x8, x8 - Device 1 function 1 enabled ; function 2 disabled 01: Reserved - (Device 1 function 1 disabled ; function 2 enabled) 00: x8,x4,x4 - Device 1 functions 1 and 2 enabled
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PEG DEFER TRAINING

CFG7	1: PEG Train immediately following xxRESETB de assertion 0: PEG Wait for BIOS for training
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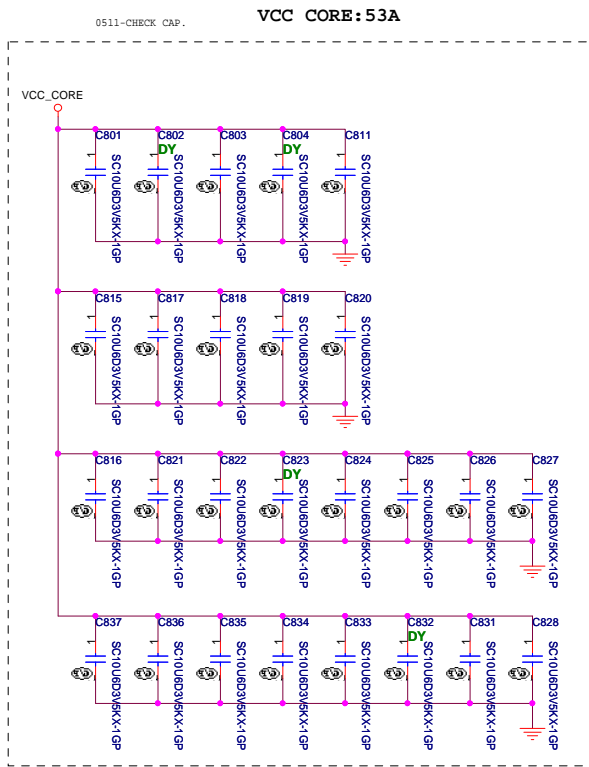


SANDY
62.10055.421
2nd = 62.10040.771

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

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VCC_CORE

AG35 VCC
AG34 VCC
AG33 VCC
AG32 VCC
AG31 VCC
AG30 VCC
AG29 VCC
AG28 VCC
AG27 VCC
AG26 VCC
AF35 VCC
AF34 VCC
AF33 VCC
AF32 VCC
AF31 VCC
AF30 VCC
AF29 VCC
AF28 VCC
AF27 VCC
AD35 VCC
AD34 VCC
AD33 VCC
AD32 VCC
AD31 VCC
AD30 VCC
AD29 VCC
AD28 VCC
AD27 VCC
AD26 VCC
AC35 VCC
AC34 VCC
AC33 VCC
AC32 VCC
AC31 VCC
AC30 VCC
AC29 VCC
AC28 VCC
AC27 VCC
AC26 VCC
AA35 VCC
AA34 VCC
AA33 VCC
AA32 VCC
AA31 VCC
AA30 VCC
AA29 VCC
AA28 VCC
AA27 VCC
AA26 VCC
Y35 VCC
Y34 VCC
Y33 VCC
Y32 VCC
Y31 VCC
Y30 VCC
Y29 VCC
Y28 VCC
Y27 VCC
Y26 VCC
Y35 VCC
Y34 VCC
Y33 VCC
Y32 VCC
Y31 VCC
Y30 VCC
Y29 VCC
Y28 VCC
Y27 VCC
Y26 VCC
U35 VCC
U34 VCC
U33 VCC
U32 VCC
U31 VCC
U30 VCC
U29 VCC
U28 VCC
U27 VCC
U26 VCC
R35 VCC
R34 VCC
R33 VCC
R32 VCC
R31 VCC
R30 VCC
R29 VCC
R28 VCC
R27 VCC
R26 VCC
P35 VCC
P34 VCC
P33 VCC
P32 VCC
P31 VCC
P30 VCC
P29 VCC
P28 VCC
P27 VCC
P26 VCC

SANDY

POWER

PEG AND DDR

CORE SUPPLY

SVID

SENSE LINES

VIDALERT#
VIDCLK
VIDSOUT

VCC_SENSE
VSS_SENSE

VCCIO_SENSE
VSSIO_SENSE

VCCIO AH13
VCCIO AH10
VCCIO AG10
VCCIO Y10
VCCIO U10
VCCIO P10
VCCIO L10
VCCIO J14
VCCIO J13
VCCIO J12
VCCIO J11
VCCIO H14
VCCIO H12
VCCIO H11
VCCIO G14
VCCIO G13
VCCIO G12
VCCIO F14
VCCIO F13
VCCIO F12
VCCIO F11
VCCIO E14
VCCIO E12

VCCIO E11
VCCIO D14
VCCIO D13
VCCIO D12
VCCIO D11
VCCIO C14
VCCIO C13
VCCIO C12
VCCIO C11
VCCIO B14
VCCIO B12
VCCIO A14
VCCIO A13
VCCIO A12
VCCIO A11

VCCIO J23

AJ29 H.CPU_SVIDALRT#
AJ30 H.CPU_SVIDCLK
AJ28 H.CPU_SVIDDAT

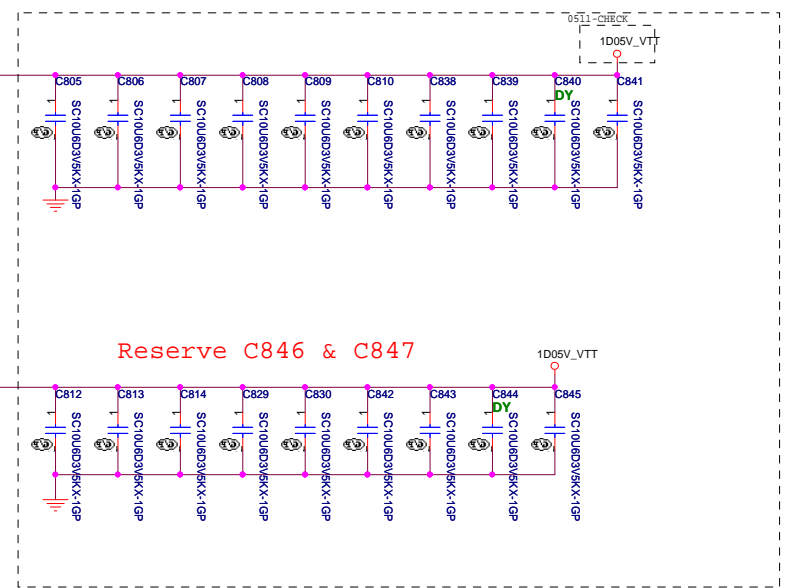
AJ35
AJ34

B10
A10

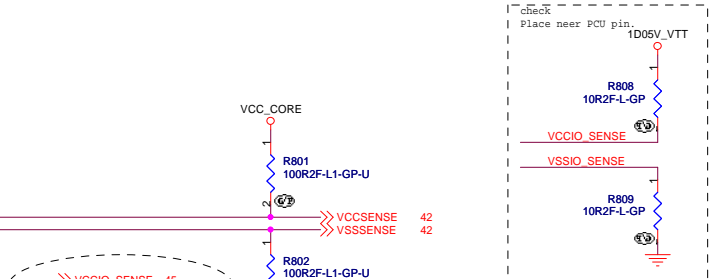
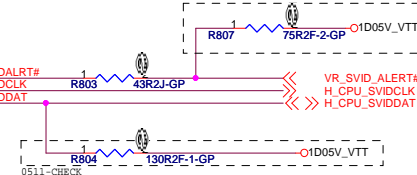


0511-CHECK CAP.

VCCIO:8.5A



For CRB VIDSOUT need to pull high 130 ohm closer to CPU and IMVP7
For CRB VIDALERT# need to pull high 75 ohm close to CPU

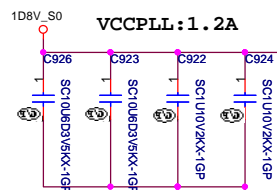
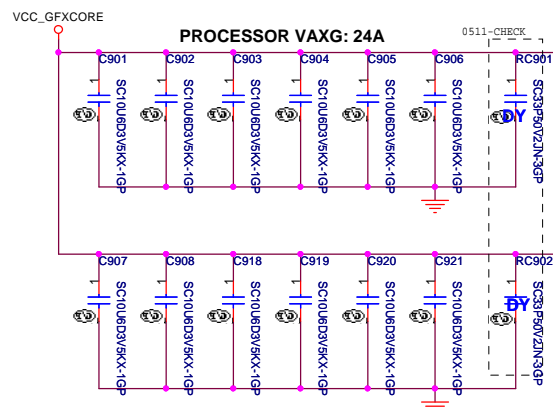


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緯創資通 Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title: CPU (VCC CORE)	
Size: Custom Date: Friday, January 06, 2012	Document Number: LA480 Rev SD
Sheet 8 of 103	

SANDY
62.10055.421
2nd = 62.10040.771

0511-CHECK CAP



POWER

CPU1G

7 OF 9

SANDY

AT24 VAXG
AT23 VAXG
AT21 VAXG
AT20 VAXG
AT18 VAXG
AT17 VAXG
AR24 VAXG
AR23 VAXG
AR21 VAXG
AR20 VAXG
AR18 VAXG
AR17 VAXG
AP24 VAXG
AP23 VAXG
AP21 VAXG
AP20 VAXG
AP18 VAXG
AP17 VAXG
AN24 VAXG
AN23 VAXG
AN21 VAXG
AN20 VAXG
AM18 VAXG
AM17 VAXG
AM24 VAXG
AM23 VAXG
AM21 VAXG
AM20 VAXG
AM18 VAXG
AM17 VAXG
AL24 VAXG
AL23 VAXG
AL21 VAXG
AL20 VAXG
AL18 VAXG
AL17 VAXG
AK24 VAXG
AK23 VAXG
AK21 VAXG
AK20 VAXG
AK18 VAXG
AK17 VAXG
AJ24 VAXG
AJ23 VAXG
AJ21 VAXG
AJ20 VAXG
AJ18 VAXG
AJ17 VAXG
AH24 VAXG
AH23 VAXG
AH21 VAXG
AH20 VAXG
AH18 VAXG
AH17 VAXG

GRAPHICS

SENSE
LINES

VREF

DDR3 - 1.5V RAILS

SA RAIL

MISC

1.8V RAIL

SANDY
62.10055.421
2nd = 62.10040.771

VAXG_SENSE
VSSAXG_SENSE

SM_VREF

VDDQ: 5A

AF7 VDDQ
AF4 VDDQ
AF1 VDDQ
AC7 VDDQ
AC4 VDDQ
AC1 VDDQ
Y7 VDDQ
Y4 VDDQ
Y1 VDDQ
U7 VDDQ
U1 VDDQ
P7 VDDQ
P4 VDDQ
P1 VDDQ

VCCSA M27
VCCSA M26
VCCSA L26
VCCSA J26
VCCSA J25
VCCSA J24
VCCSA H26
VCCSA H25

VCCSA_SENSE

FC_C22
VCCSA_VID1VCC_AXG_SENSE 42
VSS_AXG_SENSE 42

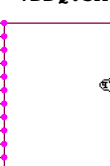
Refer to the latest Huron River Mainstream PDG
(Doc# 436735) for more details on S3 power
reduction implementation.

+V_SM_VREF_CNT should have 10 mil trace width

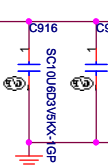
Routing Guideline:
Power from DDR_VREF_S3 and +V_SM_VREF_CNT
should have 10 mils trace width.

+V_SM_VREF_CNT 37

VDDQ: 5A



VCCA: 6A



+V0.85S - VCCSA - System Agent rail voltage can be
[0.9, 0.725, 0.8, 0.675] V for IVB
[0.9, 0.8] V for SNB

VCCSA_SENSE 48

VCCSA_SELECT0 48
VCCSA_SELECT1 48RN901
SRN1KJ-7-GP

VCC_GFXCORE

VCC_AXG_SENSE
VSS_AXG_SENSER906
100R2F-L1-GP-UR907
100R2F-L1-GP-U

1D5V_S0

<Core Design>

緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

CPU (VCC GFXCORE)

Size

A3

Document Number

LA480

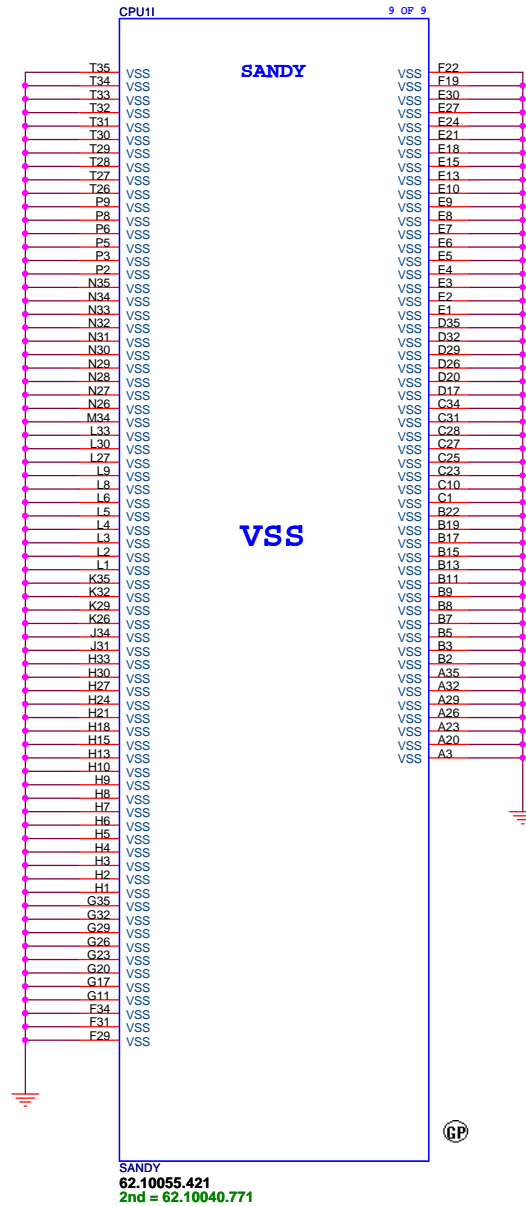
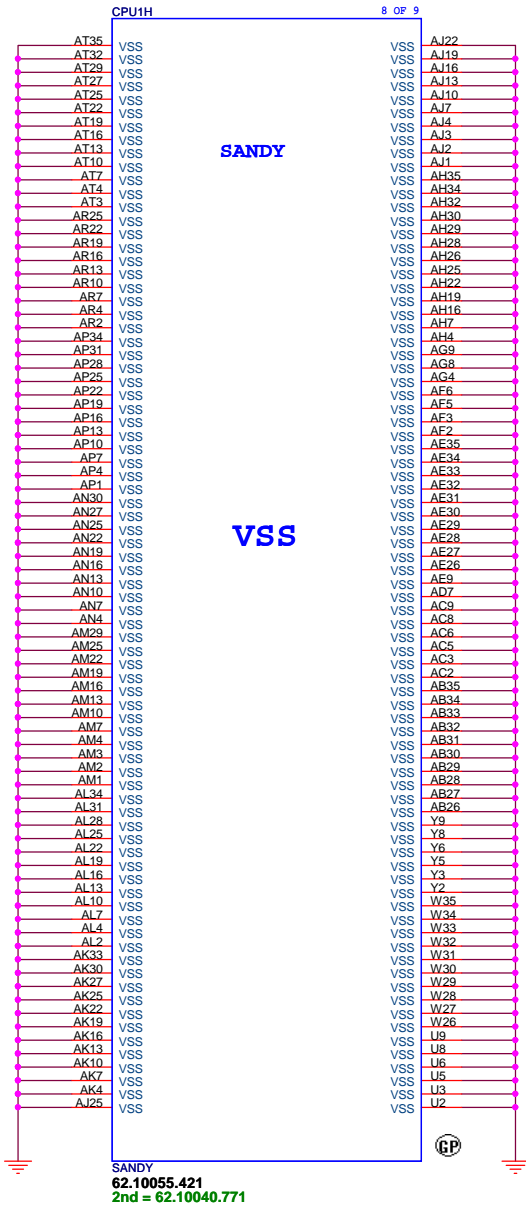
Date: Friday, January 06, 2012

Sheet 9 of 103

Rev

SD

SSID = CPU



D

C

B

A

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<Core Design>

<div><div>緯創資通</div><div>Wistron Corporation</div><div>21F,88,Sec.1,Hsin Tai Wu Rd.,Hsichih, Taipei Hsien 221, Taiwan, R.O.C</div></div>		
Title <Title>		
Size A4	Document Number LA480	Rev SD
Date: Friday, January 06, 2012	Sheet 11 of 103	

CAD Note: All VREF traces should have 20:20 mil trace geometry. Note that while 20 mil trace width is optimal, short violations is acceptable if required due to tight routing constraints.



D

C

B

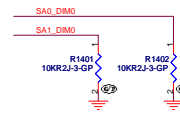
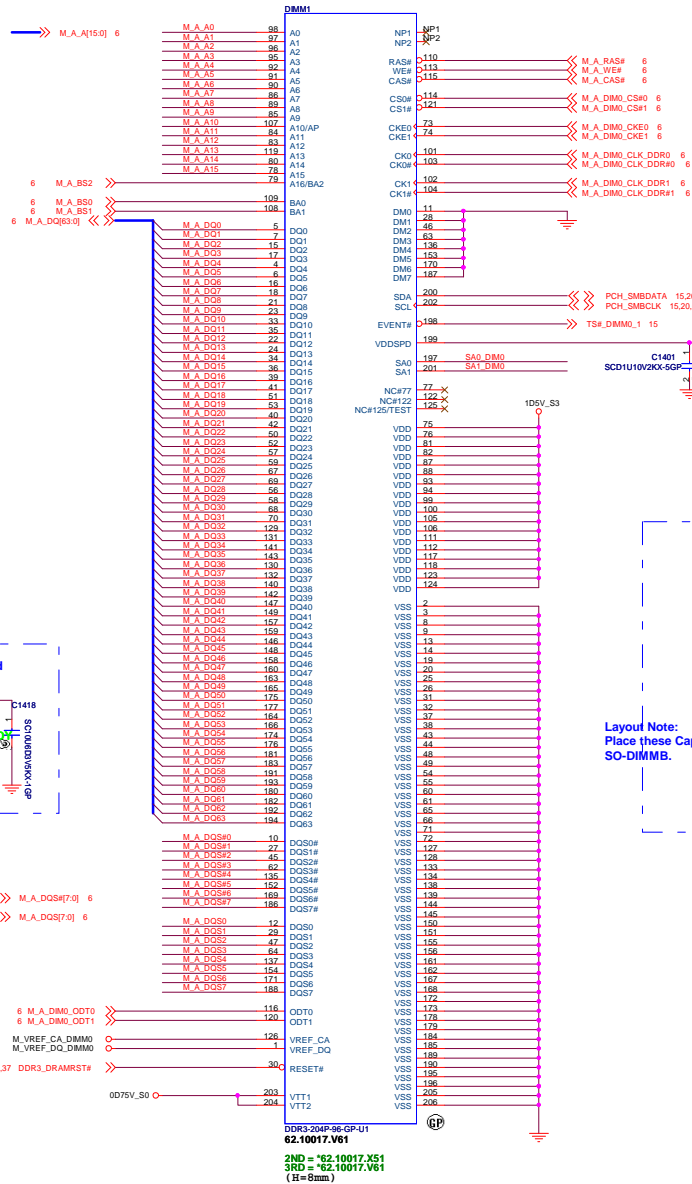
A

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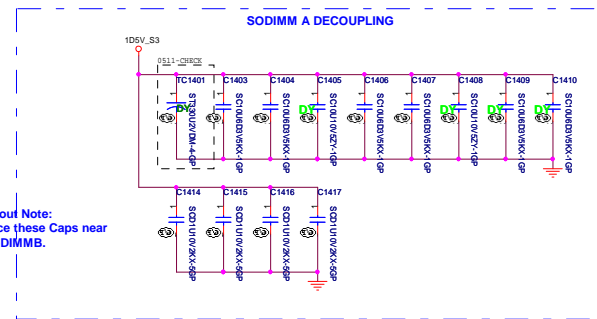
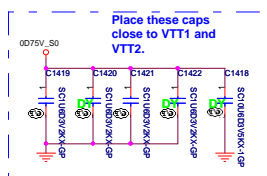
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Title <Title>		
Size A4	Document Number LA480	Rev SD
Date: Friday, January 06, 2012	Sheet 13	of 103

SSID = MEMORY



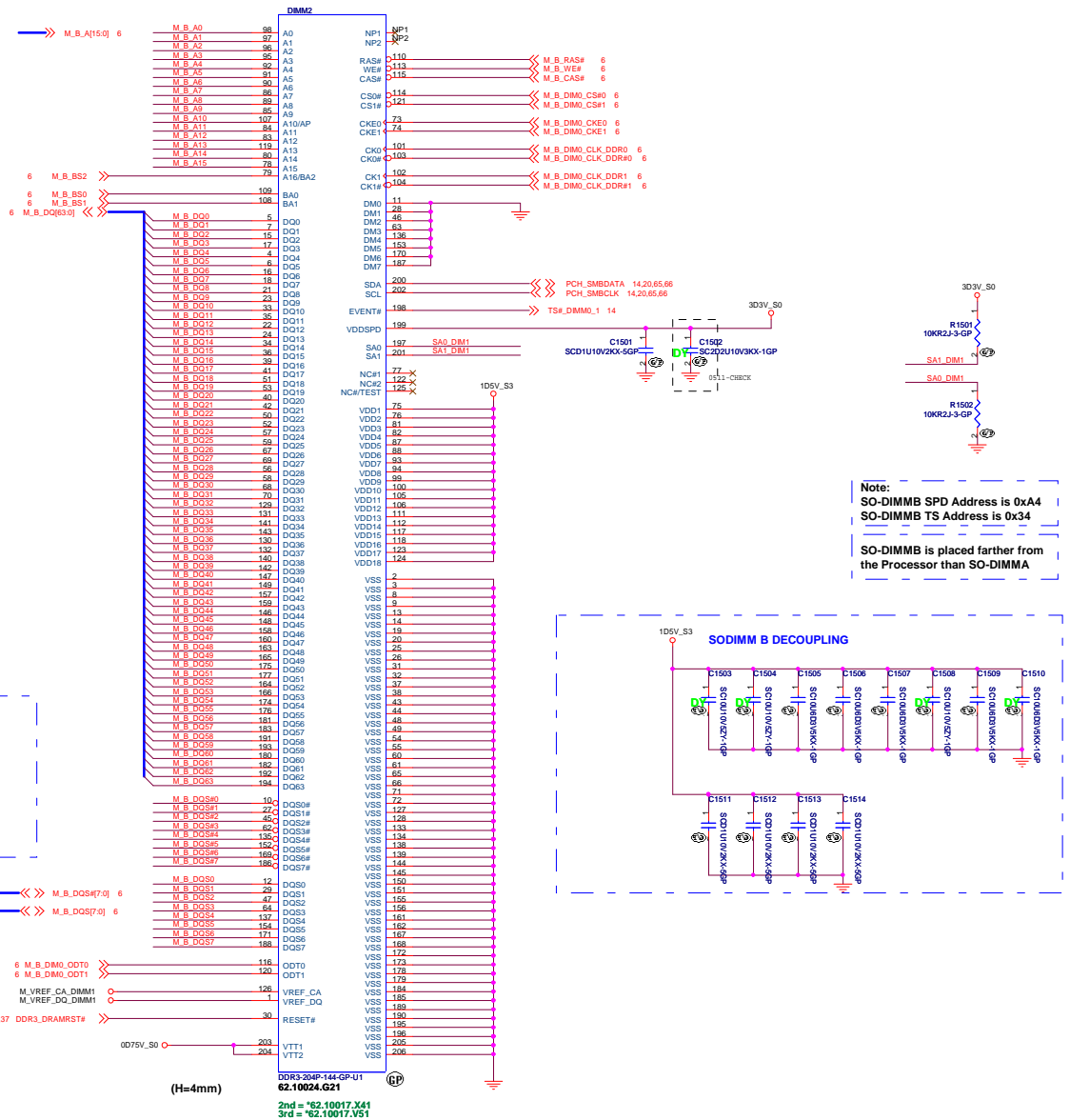
Note:
If SA0_DIM0 = 0, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA0
SO-DIMMA TS Address is 0x30

If SA0_DIM0 = 1, SA1_DIM0 = 0
SO-DIMMA SPD Address is 0xA2
SO-DIMMA TS Address is 0x32



Layout Note:
Place these Caps near
SO-DIMMB.

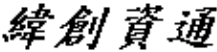
SSID = MEMORY

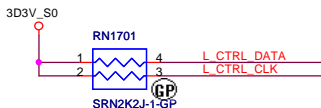


62.10017.X41
380-62.10017.V51

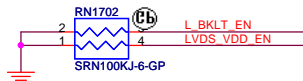
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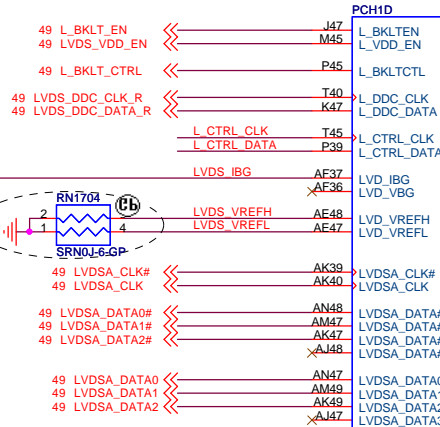
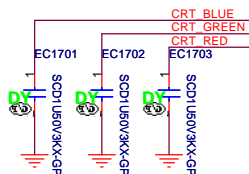
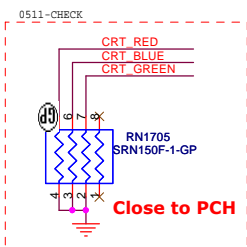
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Title			
DDR3-SODIMM2			
Size	Document Number		Rev
A4	LA480		SD
Date: Friday, January 06, 2012		Sheet 16 of	103



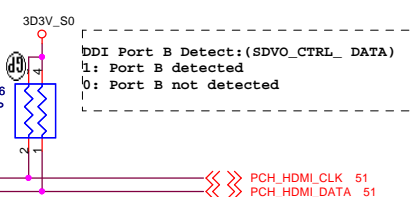
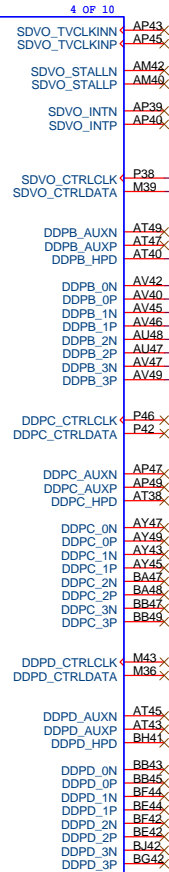
L_DDC_DATA(K47):
This signal is on the LVDS interface.
This signal needs to be left NC if eDP is
used for the local flat panel display



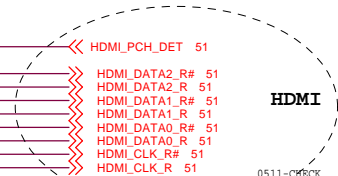
Close to PCH
Close to PCH and keep 20mil
away from other signal.



Digital Display Interface
LVDS
CART



DDI Port B Detect: (SDVO_CTRL_DATA)
1: Port B detected
0: Port B not detected

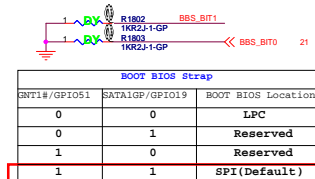
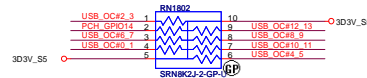
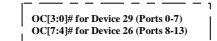
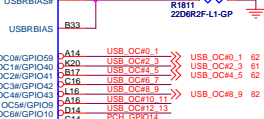
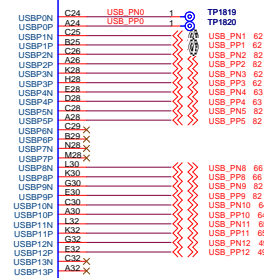
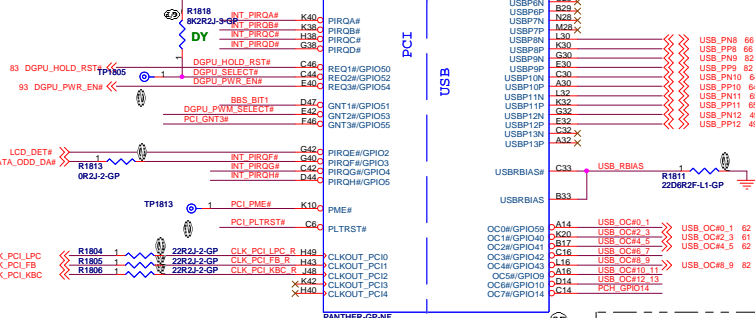
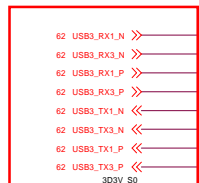
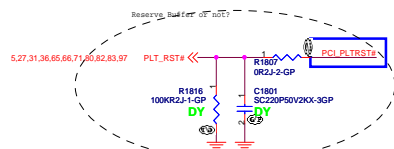
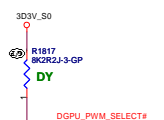
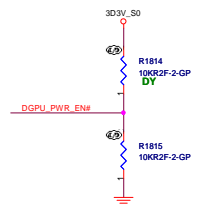
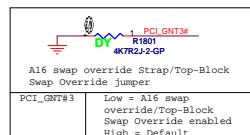
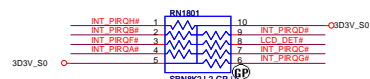


PORT	DDI PCH Pin Names	HDMI/DVI Mapping
PORT-B	DDPB_[0]P	TMDSB_DATA2#
	DDPB_[0]N	TMDSB_DATA2#
	DDPB_[1]P	TMDSB_DATA1#
	DDPB_[1]N	TMDSB_DATA1#
	DDPB_[2]P	TMDSB_DATA0#
	DDPB_[2]N	TMDSB_DATA0#
	DDPB_[3]P	TMDSB_CLK#
	DDPB_[3]N	TMDSB_CLK#
	DDPB_AUXN	NA
	DDPB_AUXP	NA
	DDPB_HPD	HDMI_HPD
	SDVO_CTRLCLK	HDMI_CTRLCLK
	SDVO_CTRLDATA	HDMI_CTRLDATA
	DDPC_CTRLCLK	
	DDPC_CTRLDATA	
	DDPD_AUXN	

Notes:
1K 0.5% 0402

The recommended value for this external resistor is 1.0 k $\pm 0.5\%$. The CRT DAC outputs may be measured when the display is completely white. If CRT DAC signal voltage value is between 665 mV to 770 mV, then the video level is within VESA specification and the reference resistor value is optimal for the motherboard design.

SSID = PCH



BOOT BIOS Strap		
GNT1#/GPIO51	SATA1GP/GPIO19	BOOT BIOS Location
0	0	LPC
0	1	Reserved
1	0	Reserved
1	1	SPI(Default)

Mini Card2 (WWAN)

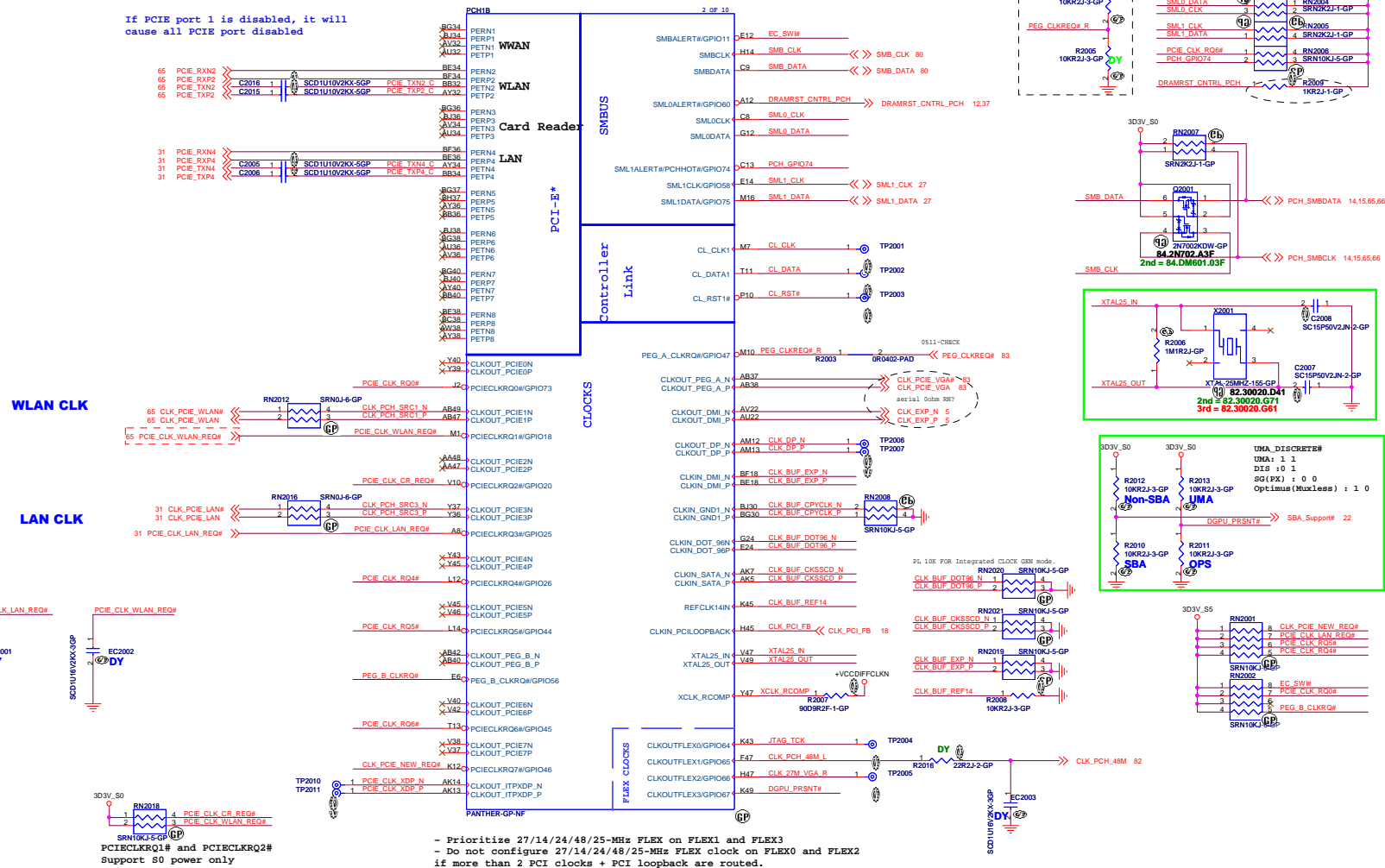
Gx8 USB Table

Pair	Device
0	X
1	USB3.0, ext port1
2	USB2.0, ext port4
3	USB3.0, ext port2
4	Bluetooth
5	CARD READER
6	X
7	X
8	3G
9	USB2.0, ext. port 3
10	Finger Print
11	Mini Card1 (WLAN)
12	CAMERA
13	X

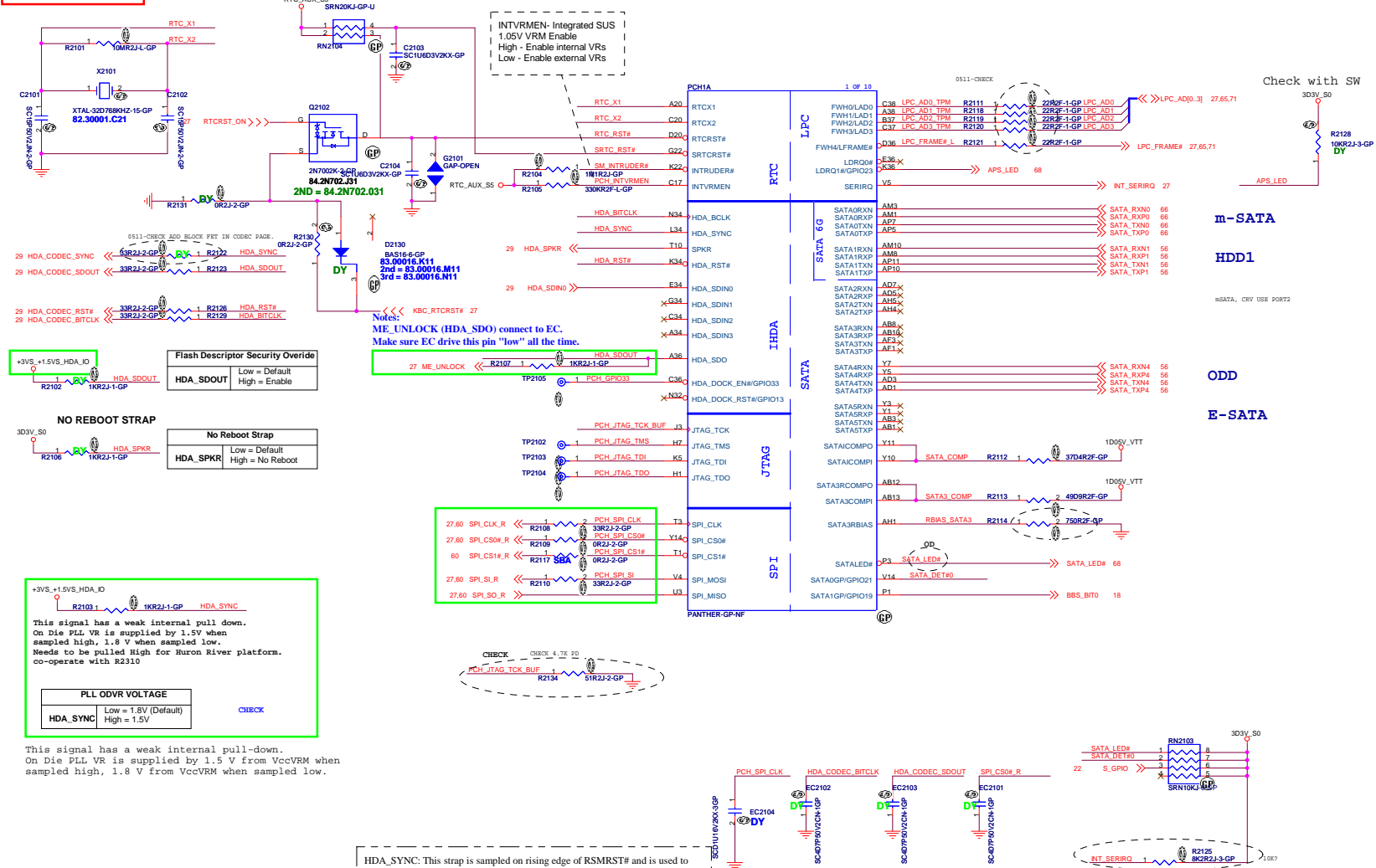
Pin	Default Port Mapping	Pin	Default Port Mapping
OC0#	Port 0, Port 1	OC4#	Port 8, Port 9
OC1#	Port 2, Port 3	OC5#	Port 10, Port 11
OC2#	Port 4, Port 5	OC6#	Port 12, Port 13
OC3#	Port 6, Port 7	OC7#	Not Used

SSID = PCH

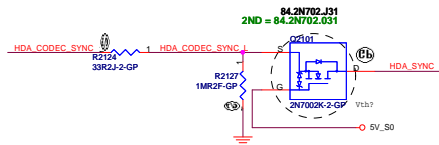
If PCIE port 1 is disabled, it will cause all PCIE port disabled



SSID = PCH



This signal has a weak internal pull-down.
On Die PLL VR is supplied by 1.5 V from VccVRM when
sampled high, 1.8 V from VccVRM when sampled low.



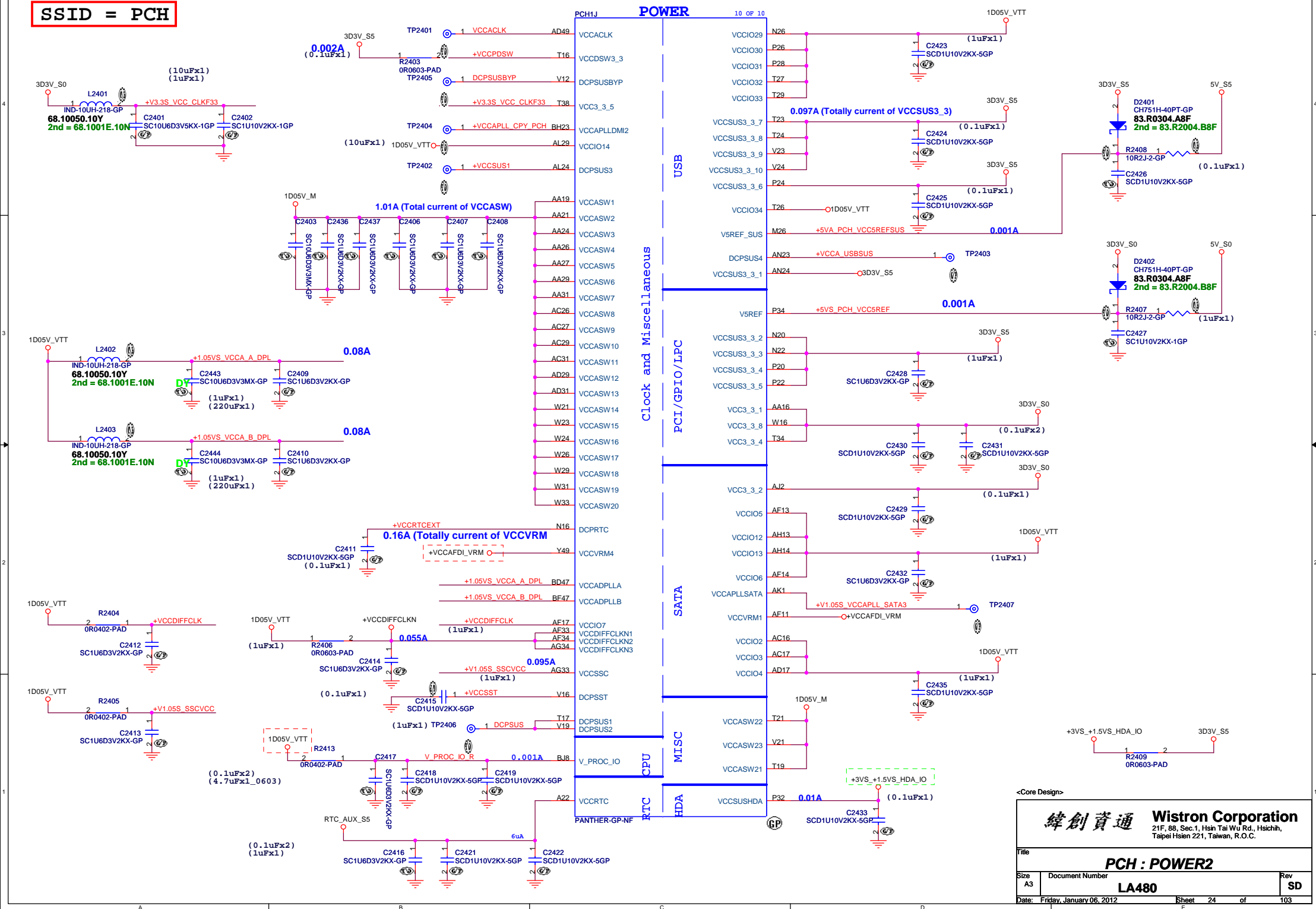
HDA_SYNC: This strap is sampled on rising edge of RSMRST# and is used to sample 1.5V VccVRM supply mode. 1K external pull-up resistor is required on this signal on the board. Signal may have leakage paths via powered off devices (Audio Codec) and hence contend with the external pull-up. A blocking FET is recommended in such a case to isolate HDA_SYNC from the Audio Codec device until after the Strap sampling is complete.

6A

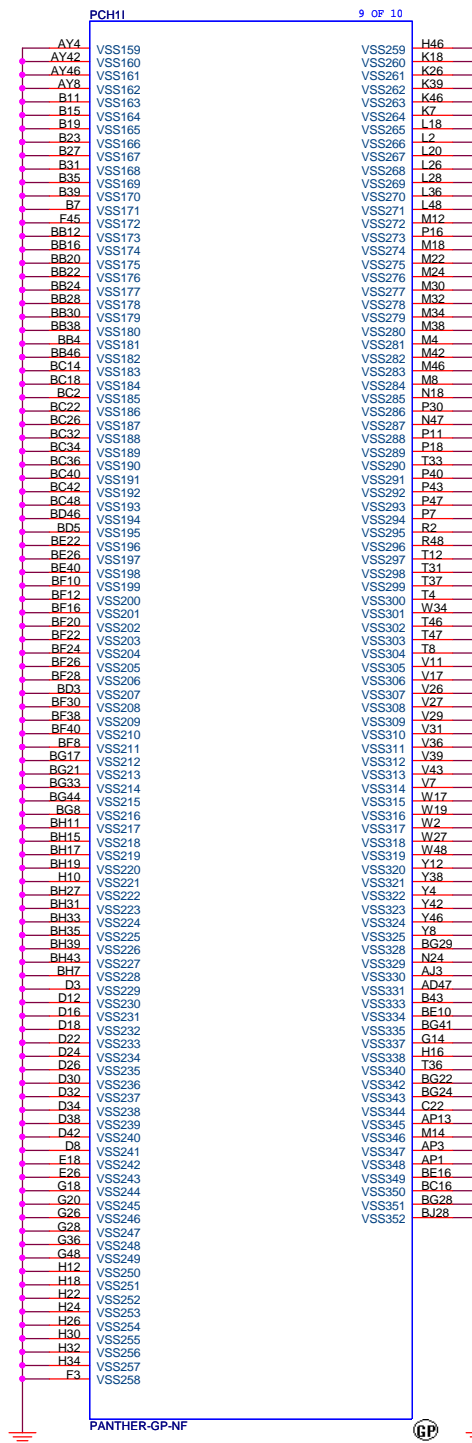
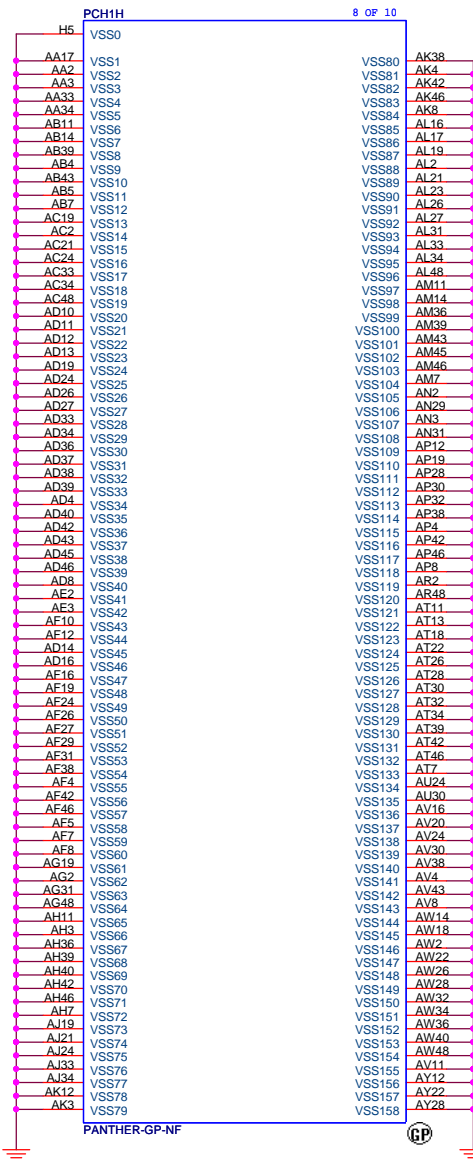


Title			
PCH : POWER1			
Size A3	Document Number LA480		Rev SD
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SSID = PCH



SSID = PCH



<Core Design>

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Title			PCH : VSS	
Size	Document Number	Rev		SD
A3	LA480			
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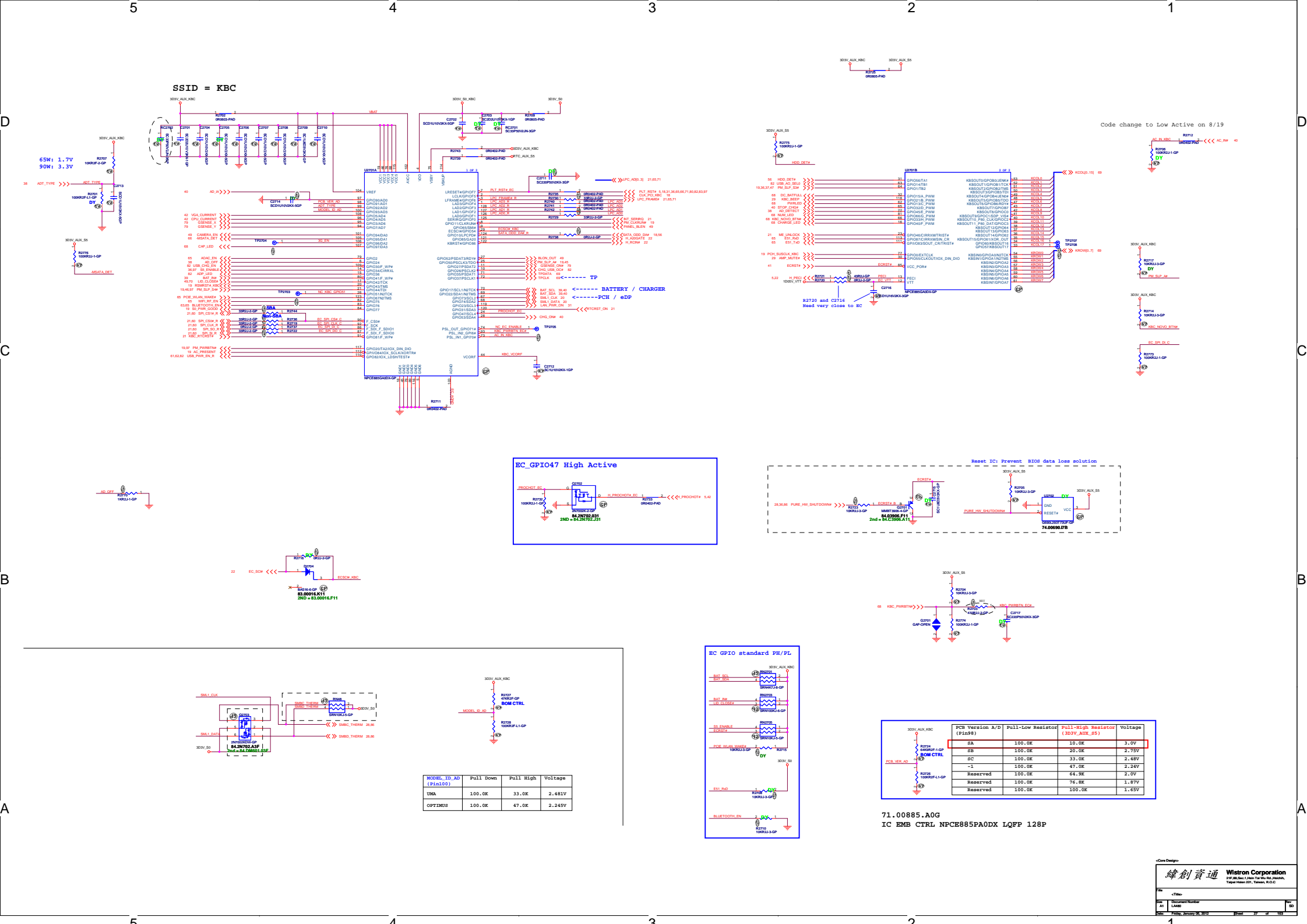
緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size A4	Document Number LA480	Rev SD
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Thermal sensor

SA 0905 change to 390p

2

Q2802

MMBT3904WT1G-GP

Q2803

SC390P50V2KX-GP

Q2804

SC390P50V2KX-GP

Q2805

SC2200P50V2KX-2GP

2200p close to smsc2103 chip

REMOTE2-

REMOTE2+

between CPU, VGA and DIMM on bottom side

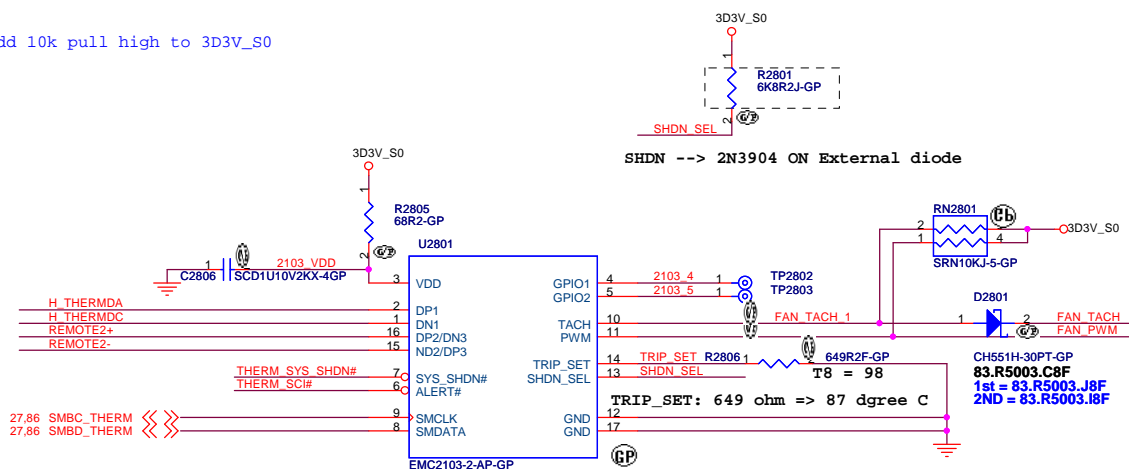
3D3V_S0

1

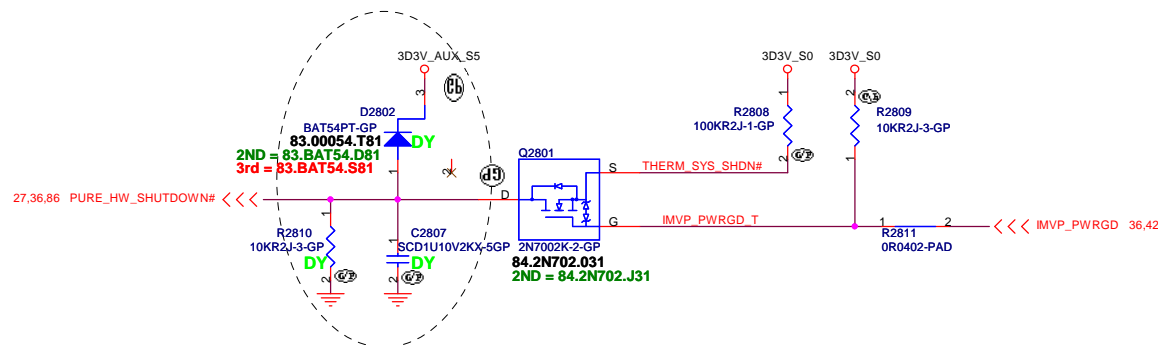
R2812
10KR2J-3-GP
DY

2

THERM_SC#



```
pin6, ALERT# OD
pin7, SYS_SHDN# OD
```



T8

1

Q2803

MMBT3904WT1G-GP1

C2808

SC2200P50V2KX-GP

C2802

SC2200P50V2KX-2GP

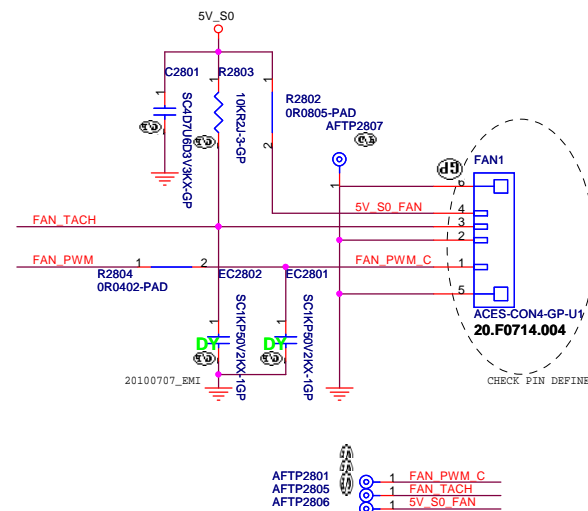
2200p close to smc2103 chip

H_THERMDA

H_THERMDC

CPU backside or inside the socket

4 WIRE PWM Fan Control circuit

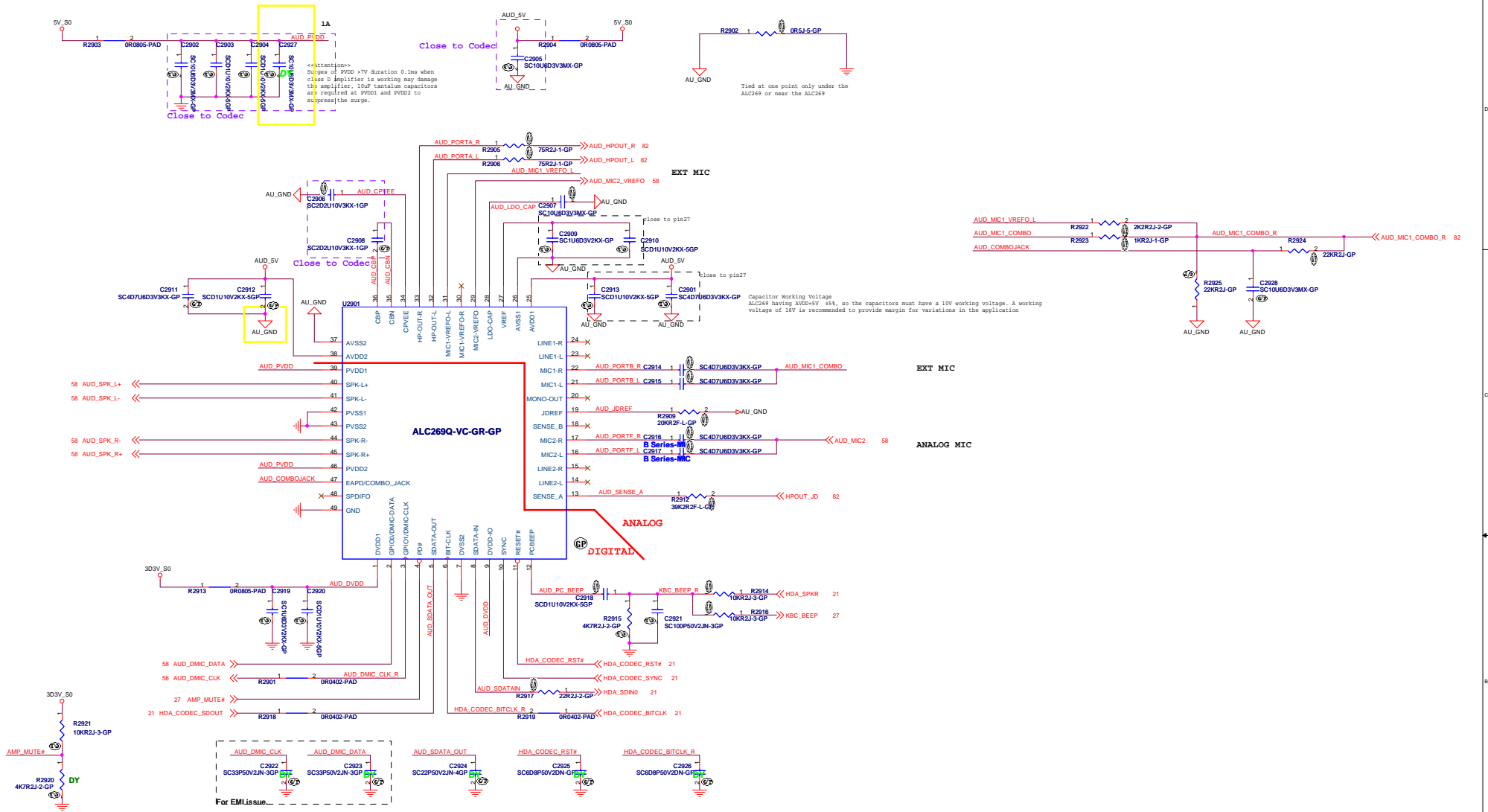


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緯創資通 **Wistron Corporation**
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Taipei Hsien 221, Taiwan, R.O.C.

Title ***THERMAL SENSOR SMSC EMC2103***

Size A3	Document Number LA480	Rev S
Date: Friday, January 06, 2012	Sheet 28 of 103	



20100705_AUD

<Core Design>

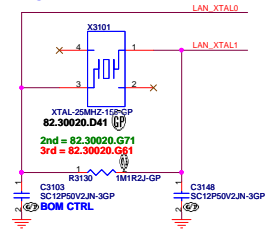
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AUDIO CODEC	
Title Size A2	Document Number LA480
Date Friday, January 06, 2012	Rev SD
Sheet 26 of 103	

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		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Reserved			
Size A4	Document Number LA480		Rev SD
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25MHz XTAL

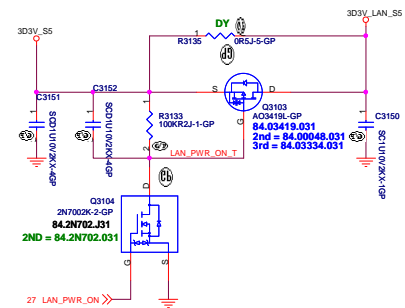
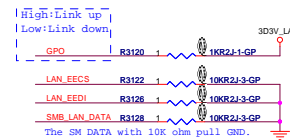
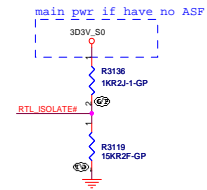
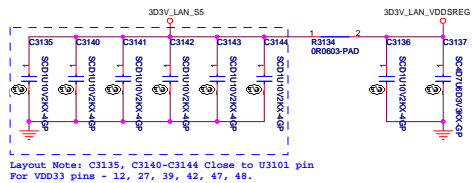
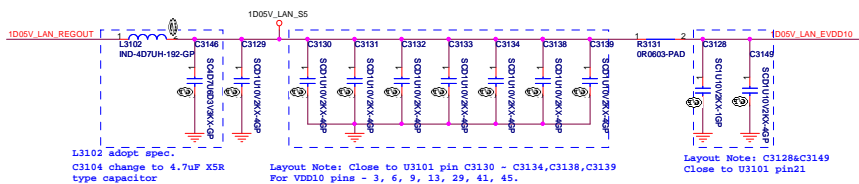
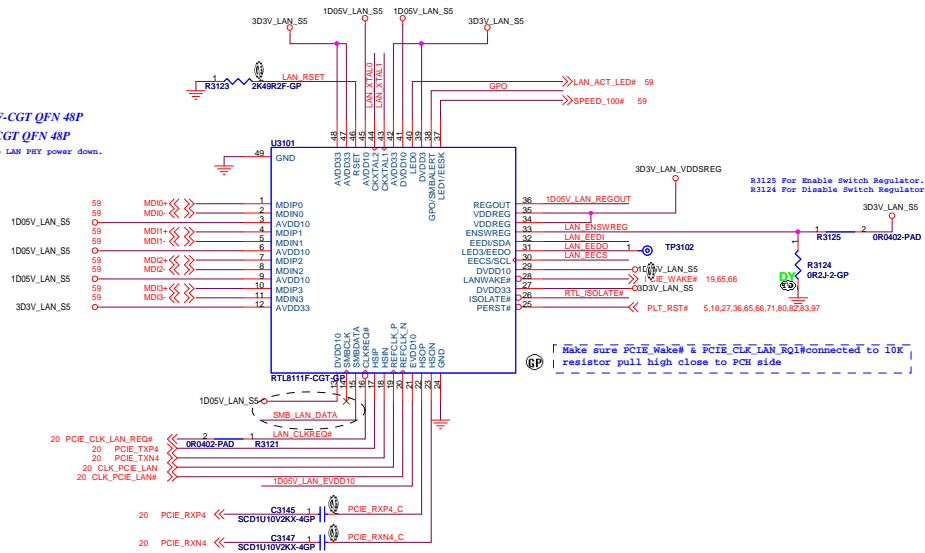


	C3103	C3148
VB480	15pF 78.15034.1FL	12pF
VB580	12pF 78.12034.1FL	12pF

71.08111.N03, IC PCIE CTRL RTL8111F-CGT QFN 48P

71.08111.J03, IC PCI-E RTL8111E-VL-CGT QFN 48P

8111F can use GPIO to inform system to do LAN PHY power down.



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<Core Design>

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Title Reserved			
Size A4	Document Number LA480		Rev SD
Date: Friday, January 06, 2012		Sheet 33 of	103

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Title Reserved			
Size A4	Document Number LA480		Rev SD
Date: Friday, January 06, 2012		Sheet 34 of	103

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Title

USB 3.0 Controller

Size
A4

Document Number

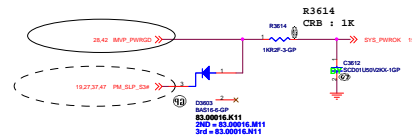
LA480

Rev
SD

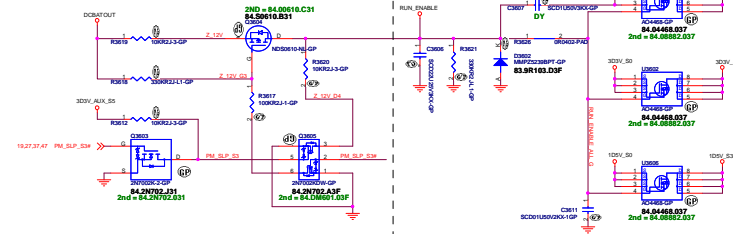
Date: Friday, January 06, 2012

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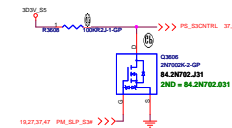
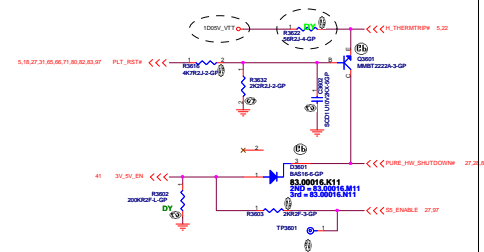
Power Sequence

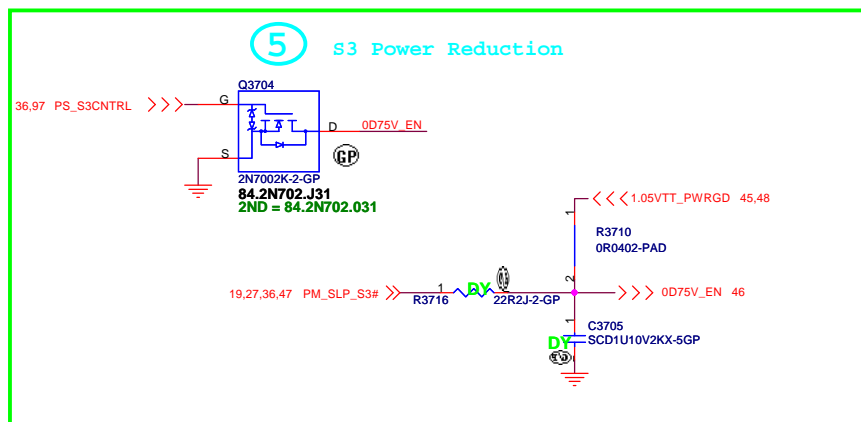
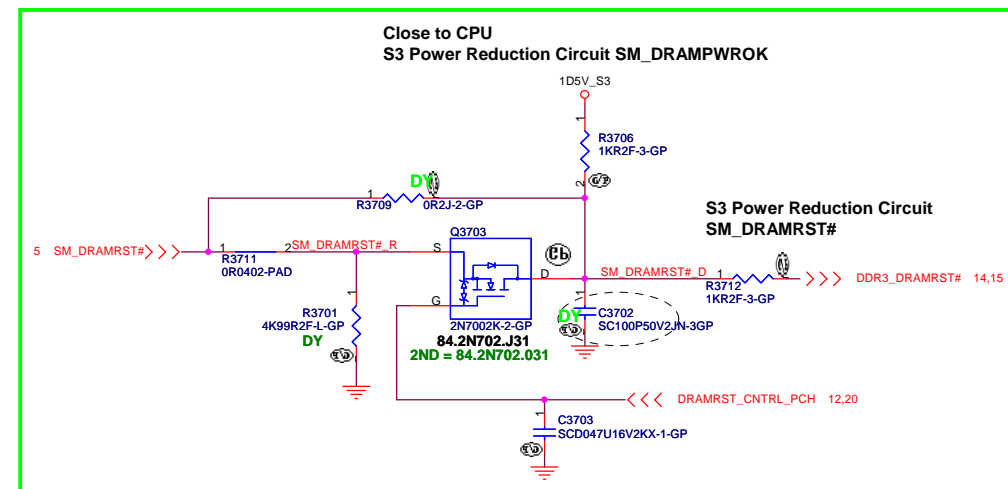
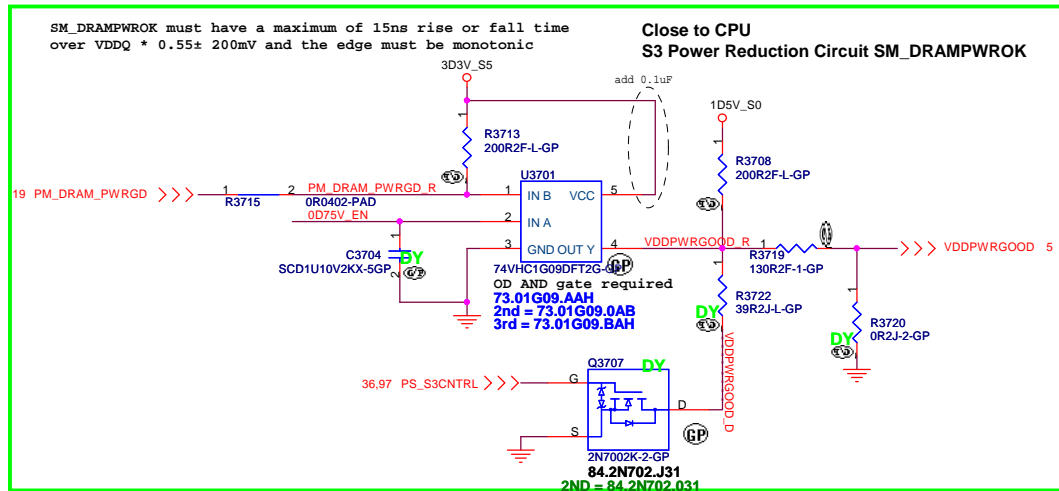
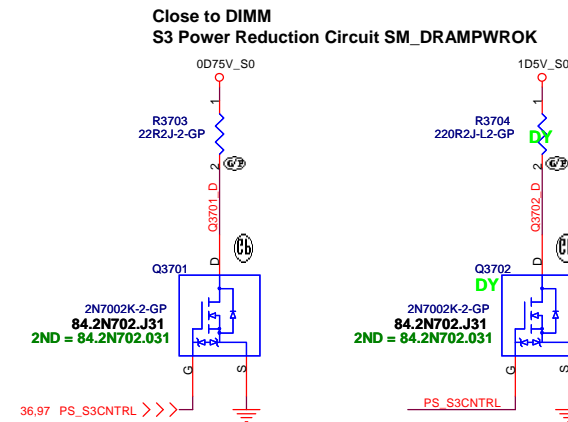
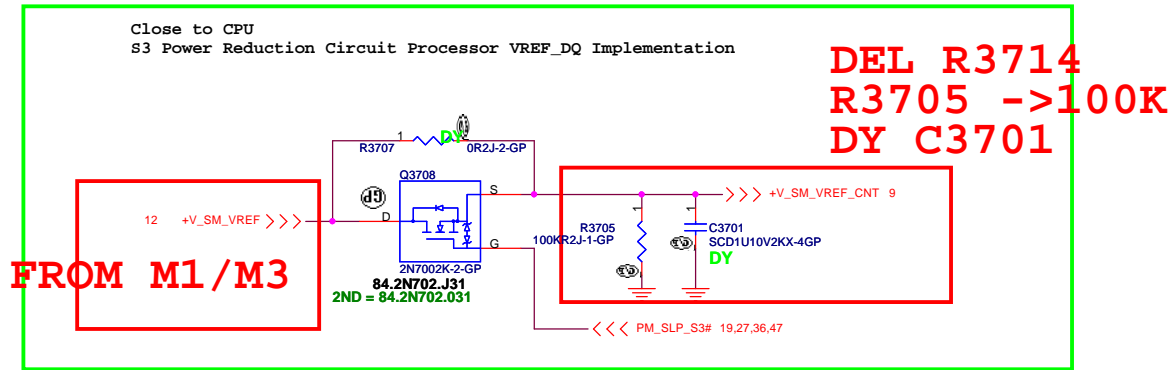


Run Power

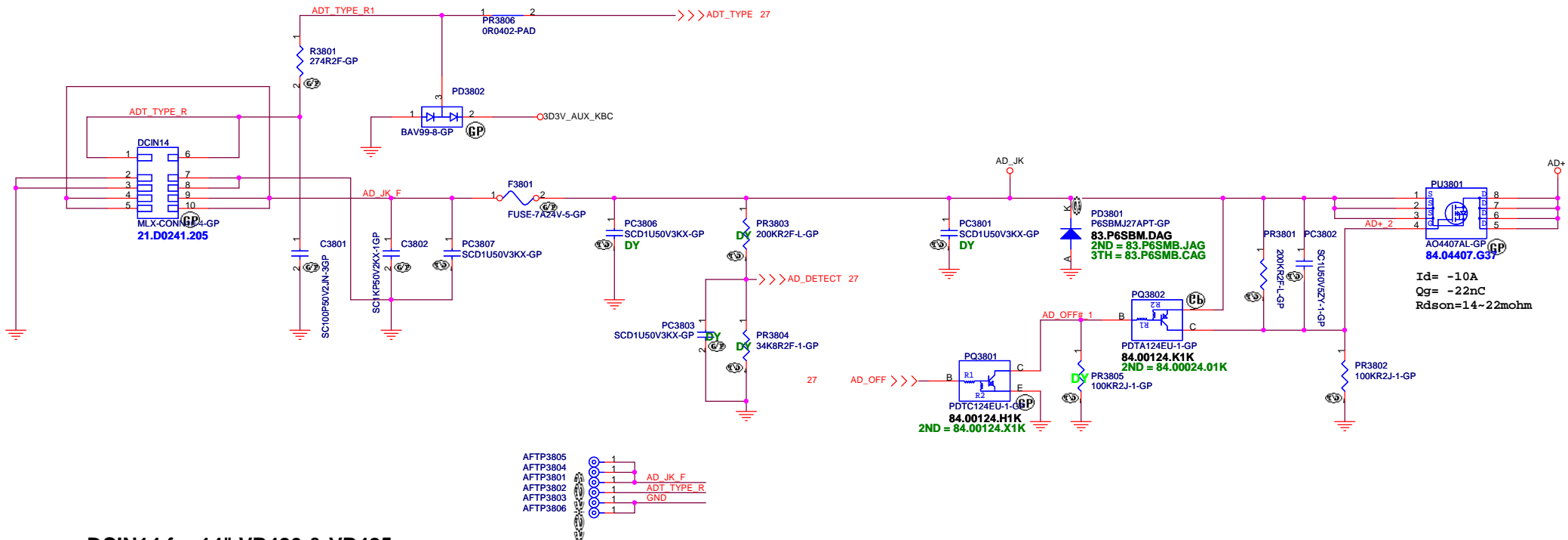


1D5V_S0
MAX Current 3000 mA
Design Current 2100 mA
Total= 11.39A

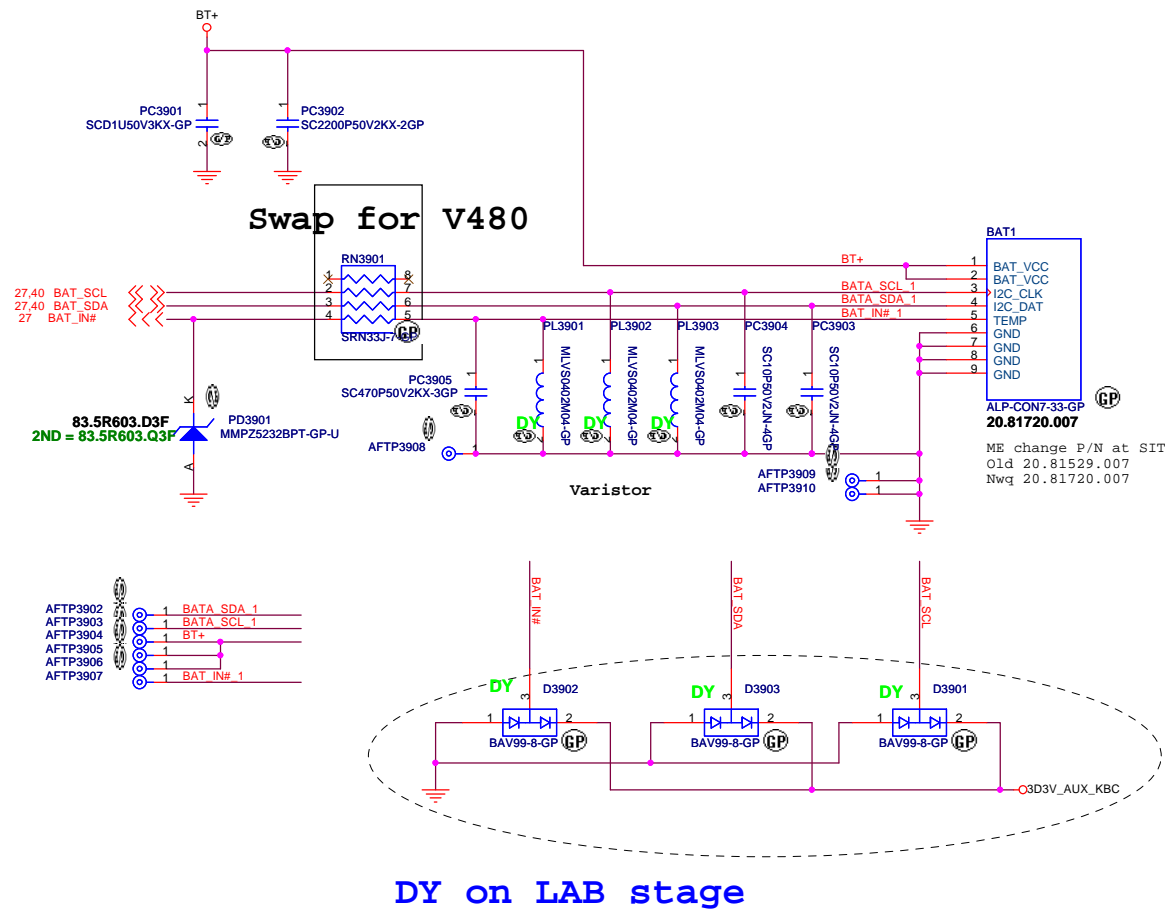




Adaptor in to generate DCBATOUT



BATTERY CONNECTOR



<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title		BATT_CONN	
Size	Document Number	LA480	Rev
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		SD	

SSID = Charger

A8(ANNIE/ASTRO)
PR4007,PR4008

AD+ total power	R1	R2
65w	64.12425.6DL	100K
80w	41.2k	100K
90w	60.4k	100K
120w	64.40425.6DL	100K

STOP_CHG#
connects to KBC

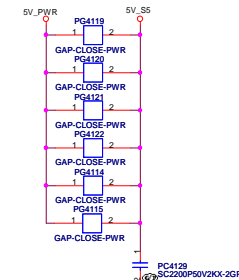
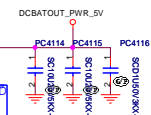
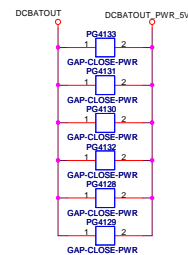
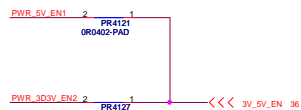
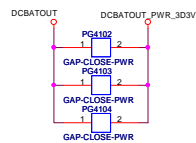
Charger Current=1.4~3.6A

<Core Design>

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Taipei Hsin 321, Taiwan, R.O.C

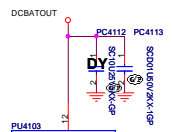
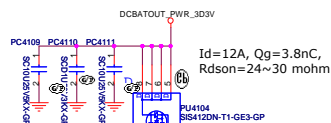
Title	<Title>		
Size	A2	Document Number	LA480
Date	Friday, January 06, 2012	Sheet	40 of 103

SSID = PWR.Plane.Regulator_5v3p3v



Design Current=5.25A
OCP>7.8A

Cyntec. 2.2uH 7.3*6.3
DCR=18~20mohm
Idc=8A, Isat=14A



Id=12A, Qg=3.8nC,
Rdson=24~30 mohm

Id=12A, Qg=3.8nC,
Rdson=24~30 mohm

Design Current=5.25A
OCP>7.8A

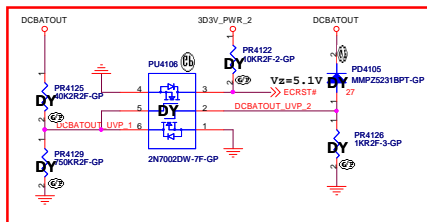
Cyntec. 3.3uH 6.5*6.9*3
DCR=28~30mohm
Idc=6A, Isat=13.5A

Id=12A, Qg=3.8nC,
Rdson=24~30 mohm

Id=16A, Qg=7.3nC,
Rdson=13.5~16.5 mohm

Close to VFB Pin (pin2)

Close to VFB Pin (pin5)



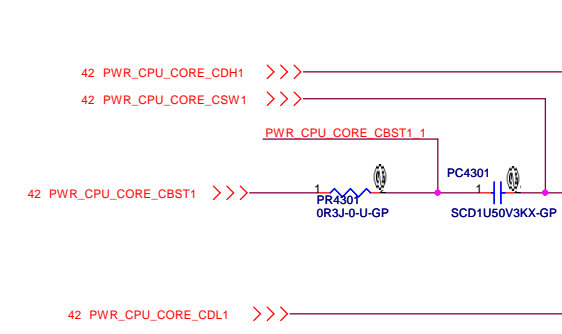
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Title TPS51123_5V_3D3V

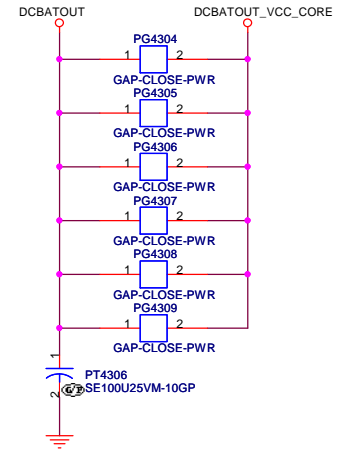
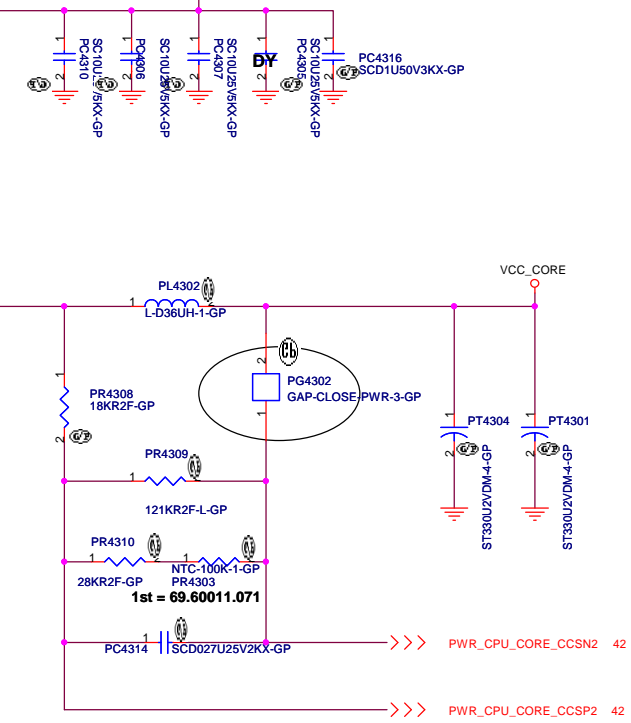
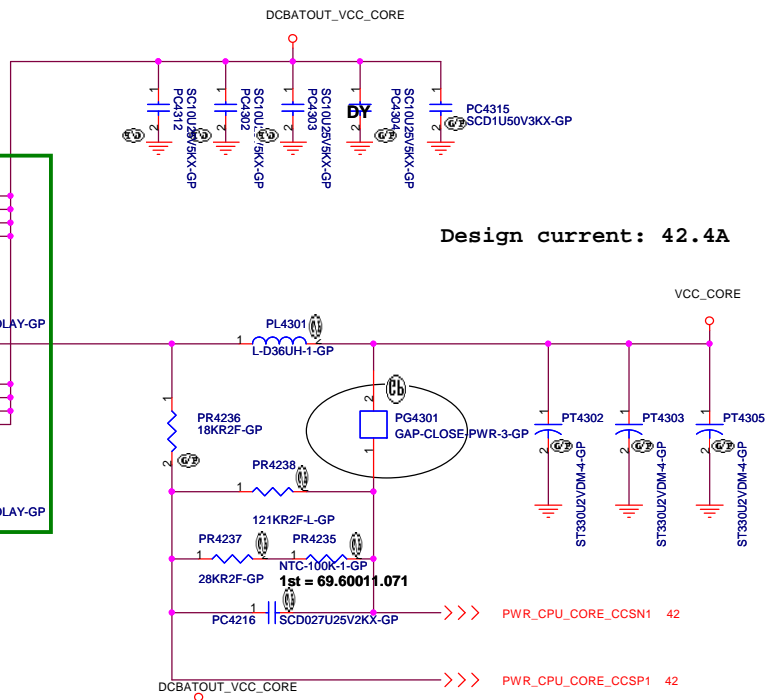
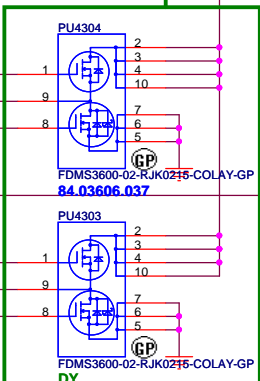
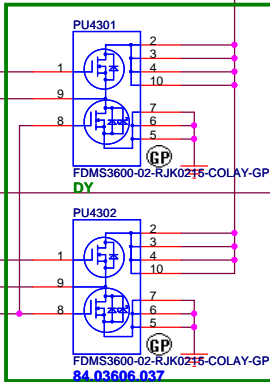
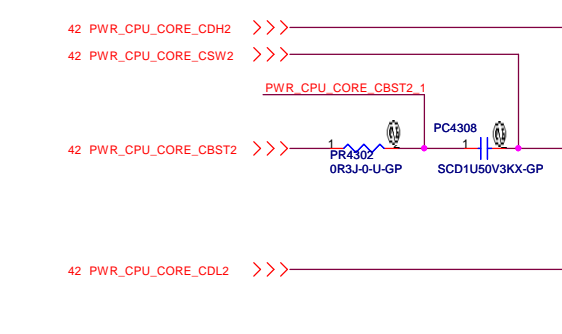
Size Document Number Rev SD

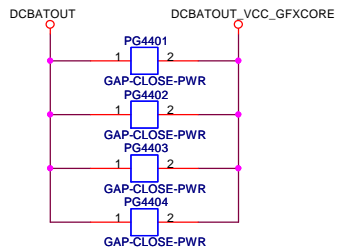
Date: Friday, January 08, 2012 Sheet 41 of 104



	Main source	2nd source
PU4301	84.03606.037 FDMS3606S-GP-U	
PU4302	84.03606.037 FDMS3606S-GP-U	
PU4303	84.03606.037 FDMS3606S-GP-U	
PU4304	84.03606.037 FDMS3606S-GP-U	

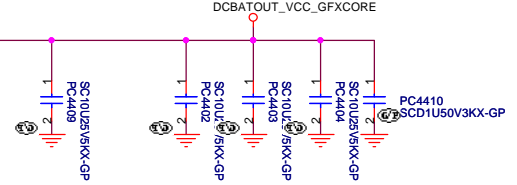
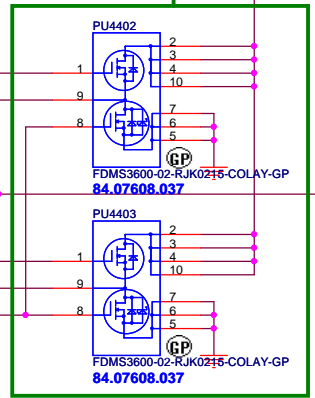
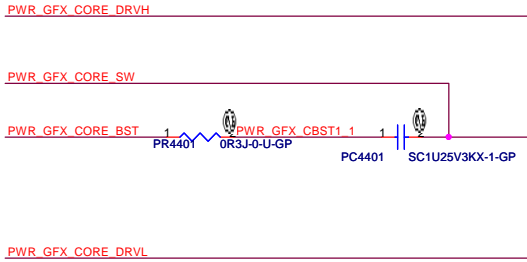
BOM control



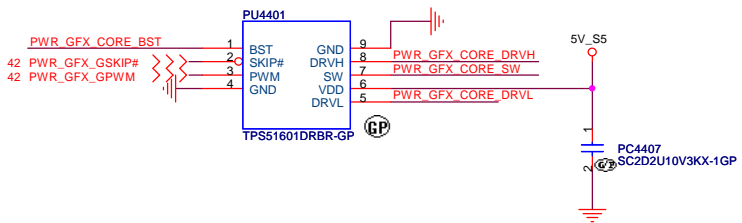
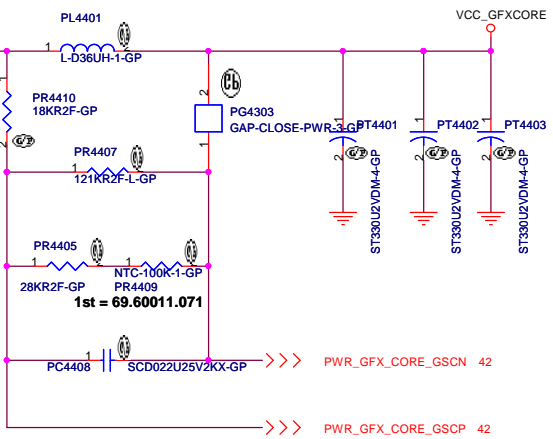


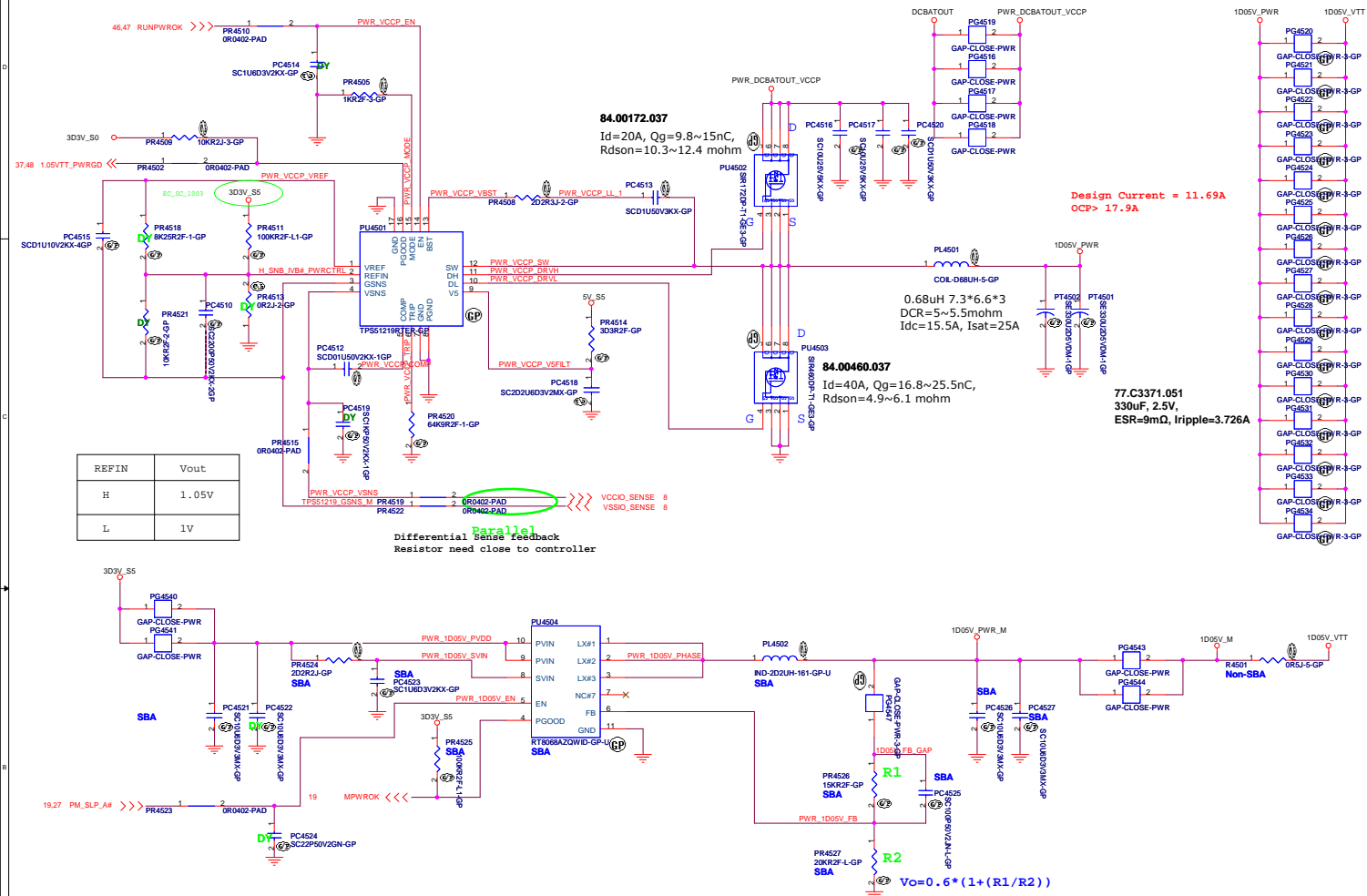
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PU4402	84.07608.037 FDMS7608S-GP	
PU4403	84.07608.037 FDMS7608S-GP	

BOM control

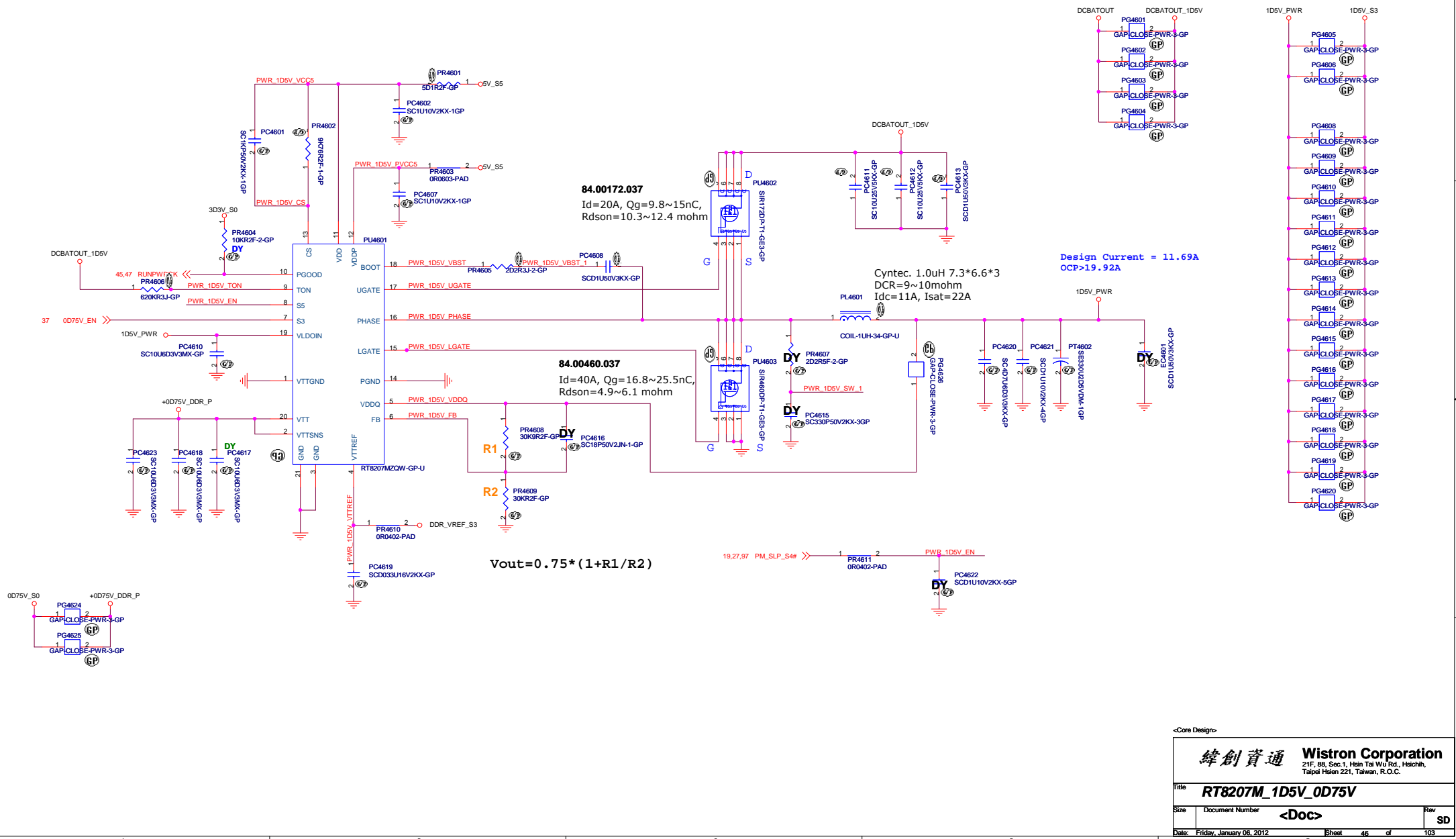


Design current: 22A

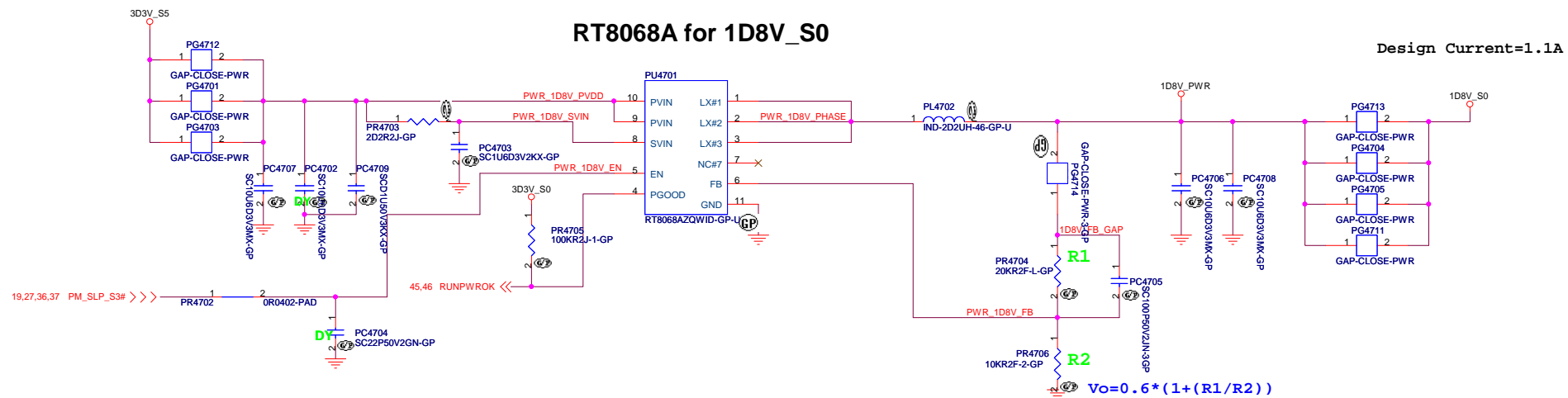


TPS51219 for 1D05V

```
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```



SSID = PWR.Plane.Regulator_1p8v



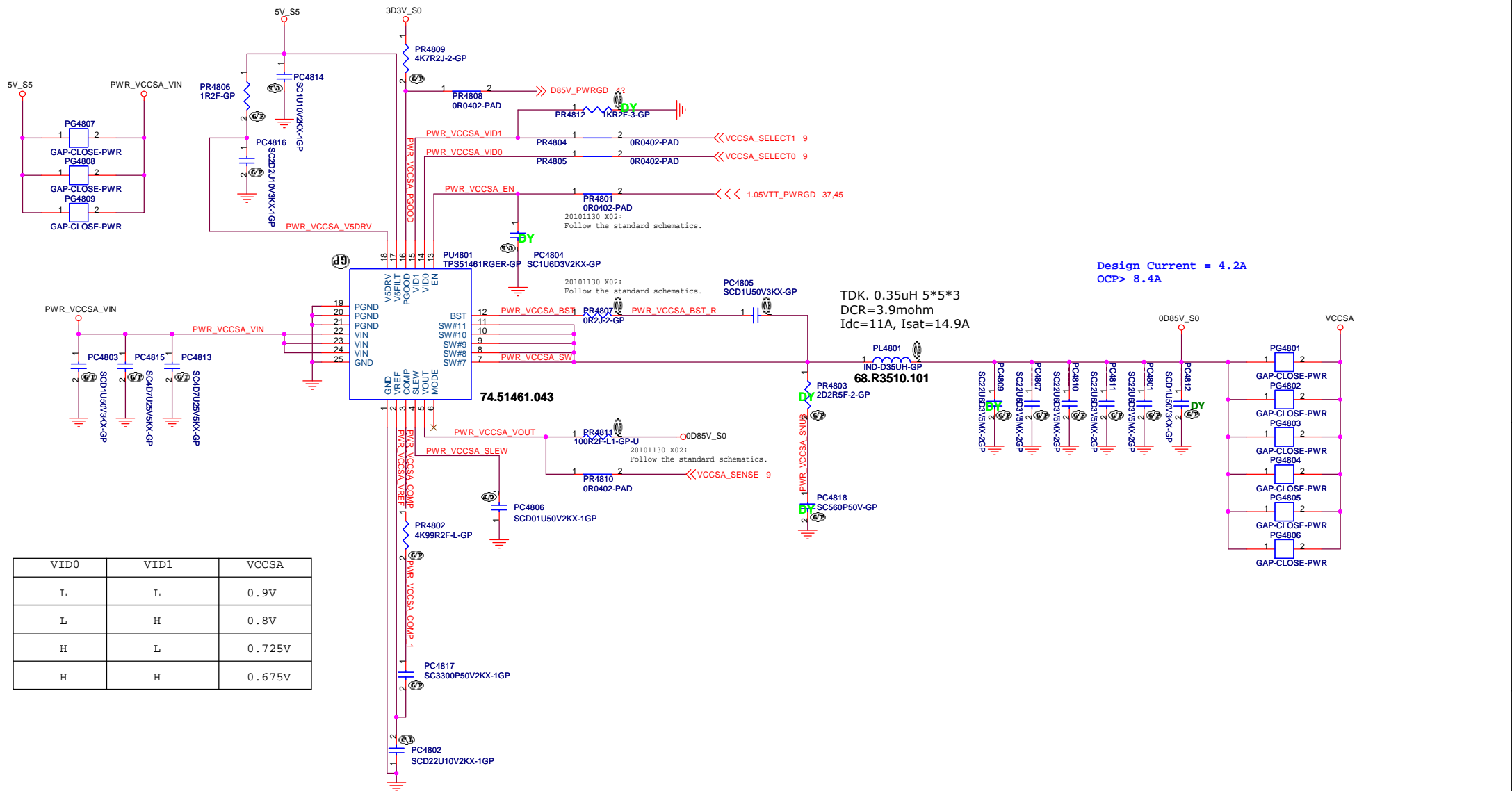
<Core Design>

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Title			PWM_1D8V_RT8015B	
Size	Document Number		Rev	SD
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TPS51461 for VCCSA



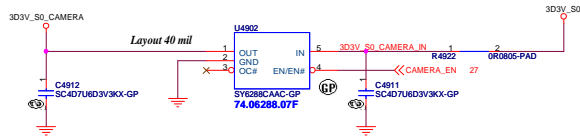
VID0	VID1	VCCSA
L	L	0.9V
L	H	0.8V
H	L	0.725V
H	H	0.675V

SSID = VIDEO

LVDS connector

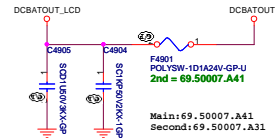
LCD / Inverter Connector

CAMERA POWER

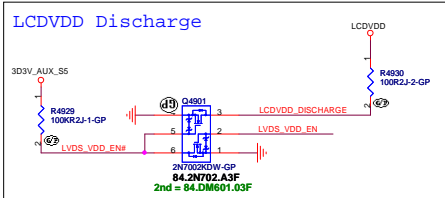


SILERGY	74.06288.07F	SY6288CAAC	High Active
DIODES	74.02171.07F	AP2171WG-7	High Active
UPI	74.07534.A7F	OBS	High Active
GMT	74.05240.A7F	OBS	High Active

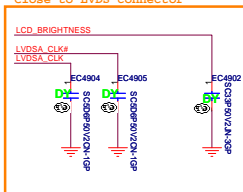
LCD POWER



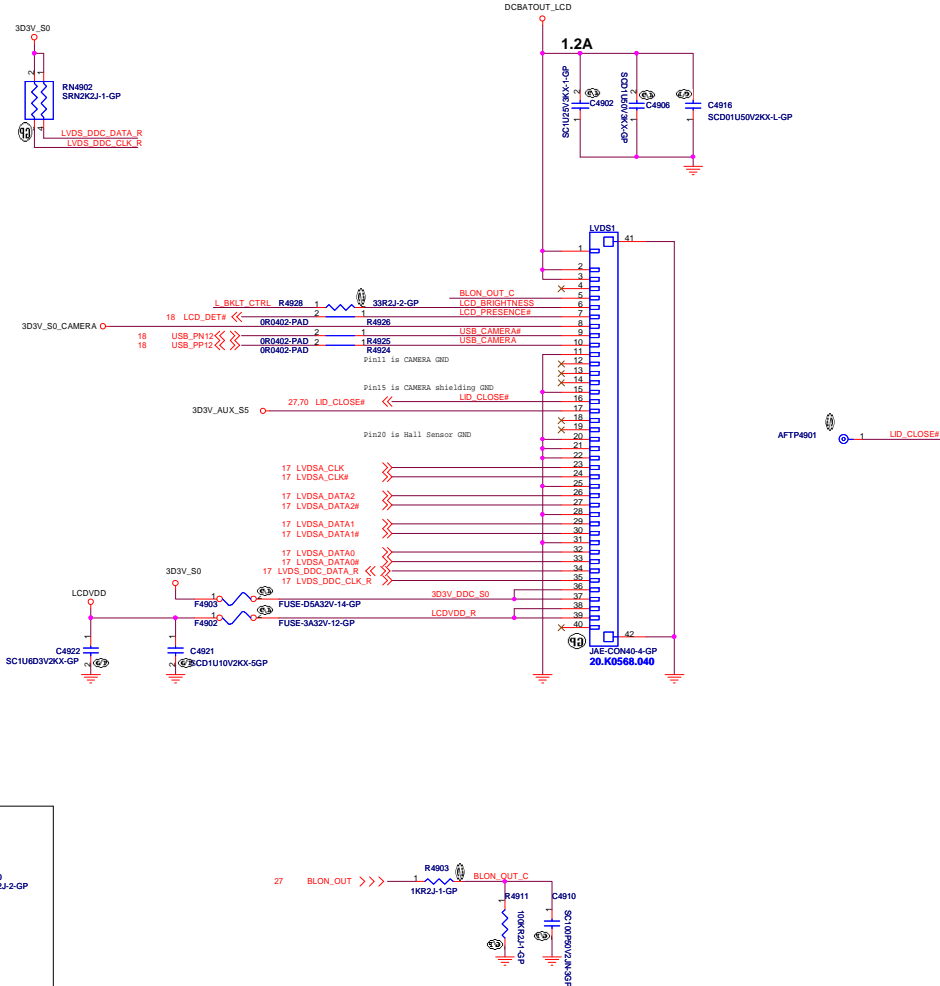
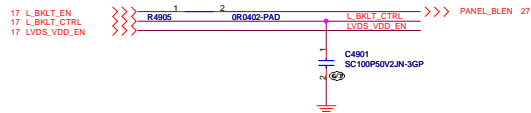
Main: 69.50007.A41
Second: 69.50007.A31



For EMI request
Close to LVDS connector



Panel BL brightness/Power En/BL En

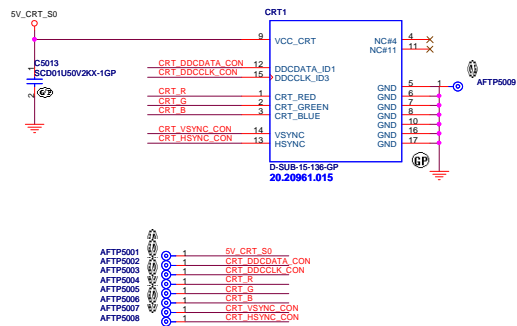


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Taippei Hsien 221, Taiwan, R.O.C.

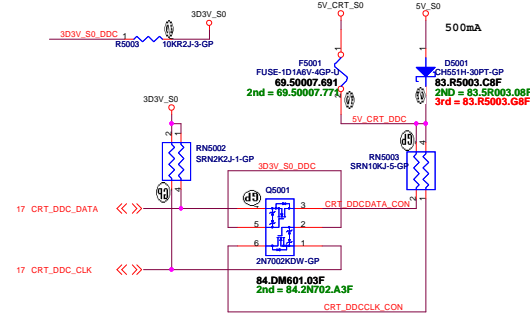
File	LCD Connector	
Size	Document Number	Rev
A2	LA480	SD
Date:	Friday, January 06, 2012	Sheet 48 of 103

CRT connector

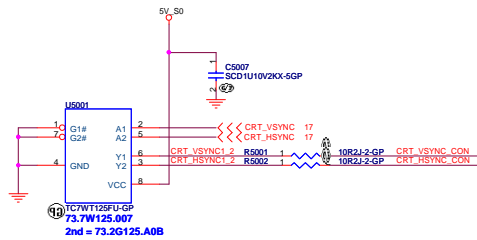


CRT DDCDATA & DDCCLK level shift

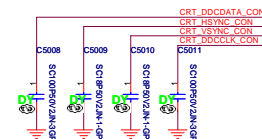
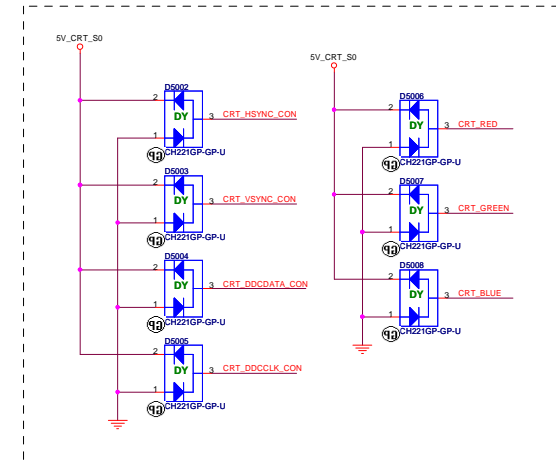
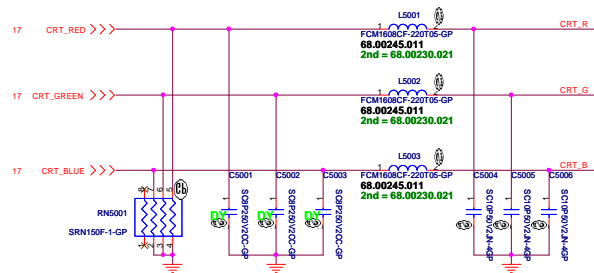
Pull High 5V Design on CRT Board



CRT Hsync & Vsync level shift



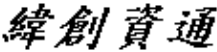
CRT RGB



<Core Design>

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<Core Design>

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Title			
eDP			
Size A4	Document Number LA480		Rev SD
Date: Friday, January 06, 2012		Sheet 52 of	103

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Title			
S-VIDEO			
Size A4	Document Number LA480		Rev SD
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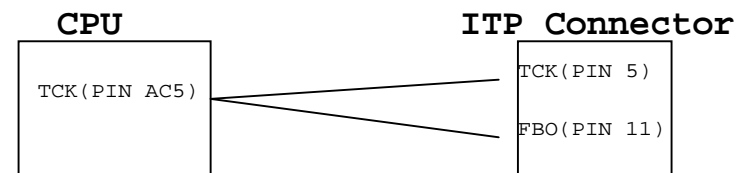
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Title Reserved			
Size A4	Document Number LA480		Rev SD
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SSID = User.Interface

ITP Connector

H_CPURST# use pull-up Resistor close
ITP connector 500 mil (max),
others place near CPU side.



<Core Design>

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Title

ITP

Size
A4

Document Number

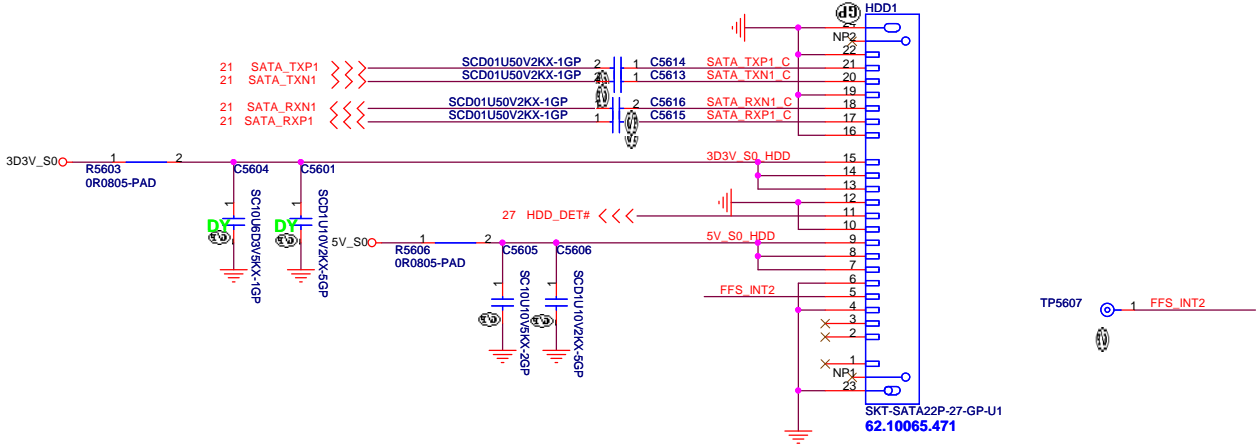
LA480

Rev
SD

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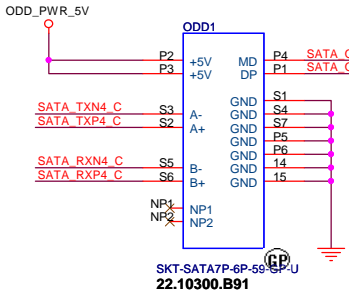
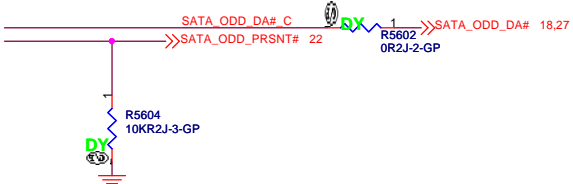
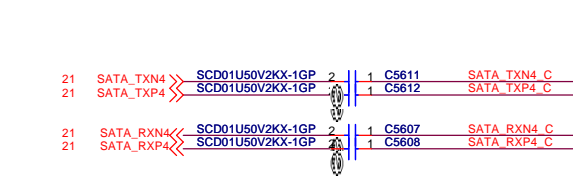
SATA HDD Connector



ODD Connector

SATA_RX- and SATA_RX+ Trace
Length match within 20 mil

Mars:
Exchange ODD and ESATA differential pair each other.

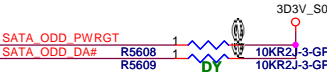
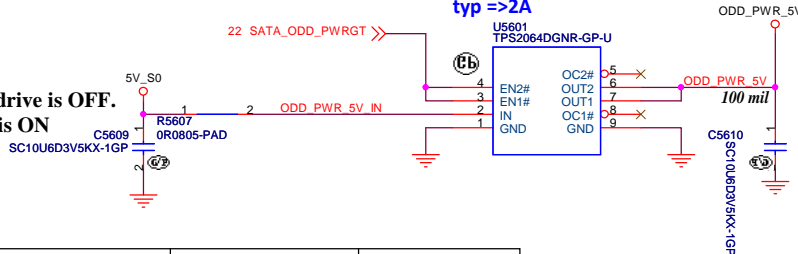


When the drive is powered on, the FET to the MD/DA pin drive is OFF.
When the drive is powered off, the FET to the MD/DA pin is ON

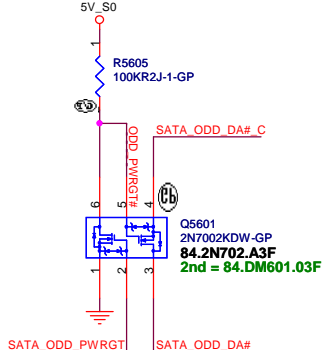
- 74.02069.079 TI TPS2069DGNR MSOP 8P
- 74.07534.D79 UPI UP7534PRA8-15 MSOP 8P
- 74.00547.C79 GMT G547F1P81U MSOP 8P (OBS)
- 74.07534.A79 UPI UP7534ARA8-15 MSOP8P

SATA Zero Power ODD

Current limit
Active High
typ =>2A



SUPPORT ZERO SATA ODD



TI	74.02069.079	TPS2069DGNR	High Active
DIODES		AP2171WG-7	High Active
UPI	74.07534.A7F	OBS	High Active

<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

Title

HDD/ODD

Size

A3

Document Number

LA480

Date

Friday, January 06, 2012

Sheet

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of

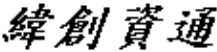
103

Rev

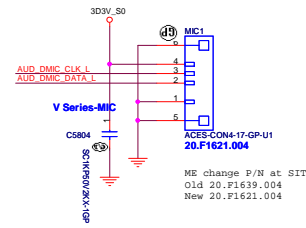
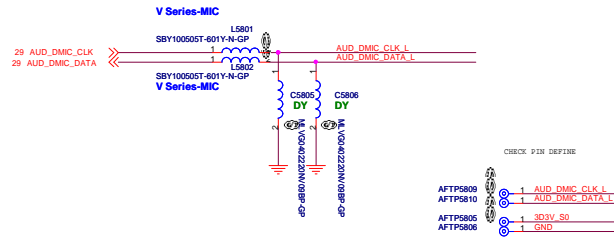
SD

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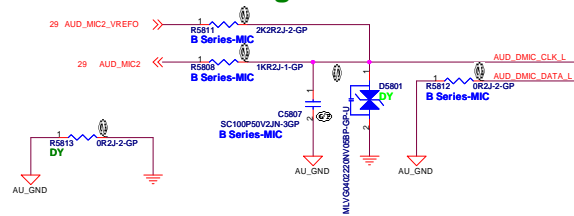
<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title E-SATA+USB			
Size A4	Document Number LA480		Rev SD
Date: Friday, January 06, 2012		Sheet 57 of	103

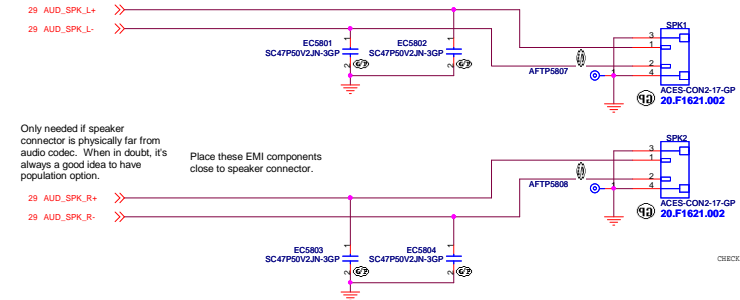
Int. Digital MIC for V series



Int. Mono Analog MIC for B series



INTERNAL STEREO SPEAKERS



Only needed if speaker connector is physically far from audio codec. When in doubt, it's always a good idea to have population option.

Place these EMI components close to speaker connector.

CHECK PIN DEFINE, RIGHT? LEFT?

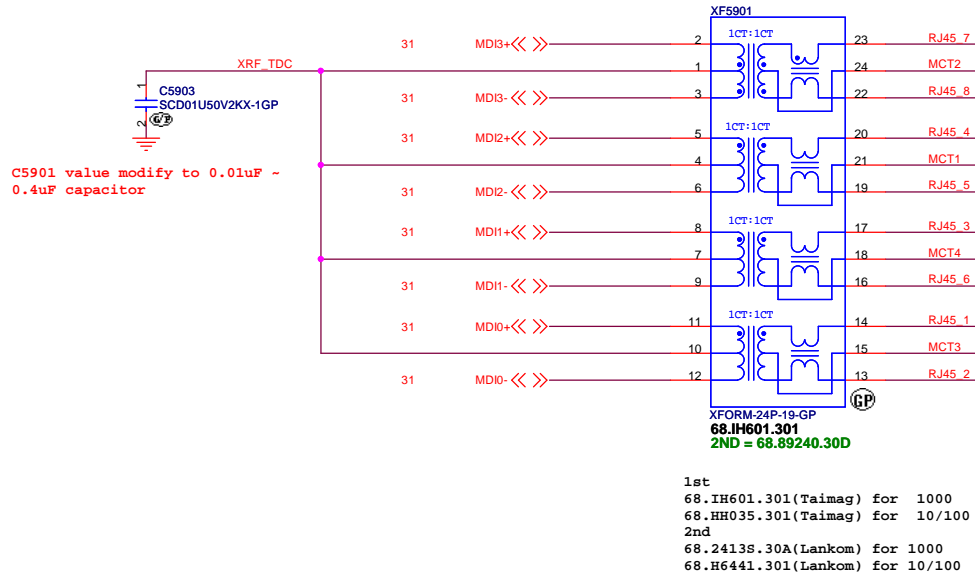
AFTP5801 1 AUD_SPK_L+
AFTP5802 1 AUD_SPK_L-
AFTP5803 1 AUD_SPK_R+
AFTP5804 1 AUD_SPK_R-

Table 58.1 - Bi-direction ESD multi-source

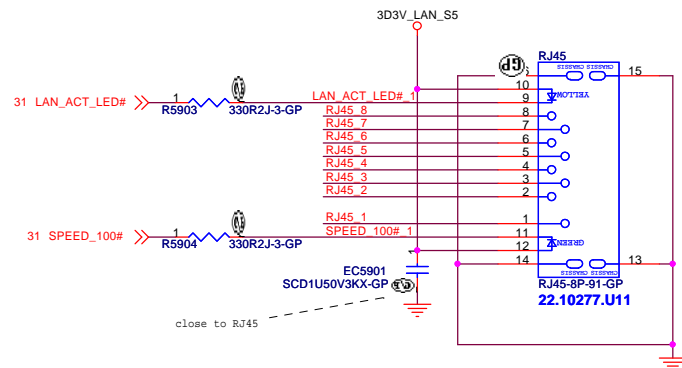
Supplier	Description	Lenovo P/N	Wistron P/N
ROHM	RSB5.6SMT2R	N/A	83.RSB56.B.
ON SEMI	ESD5B5.0ST1G	N/A	83.ESD5B.0.
NXP	PESD5V0S1BB	N/A	83.0005V.0A

FOR CO-LAY

GIGA Lan Transformer



LAN Connector



TVS

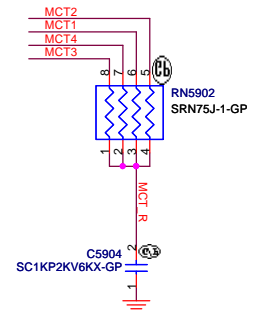
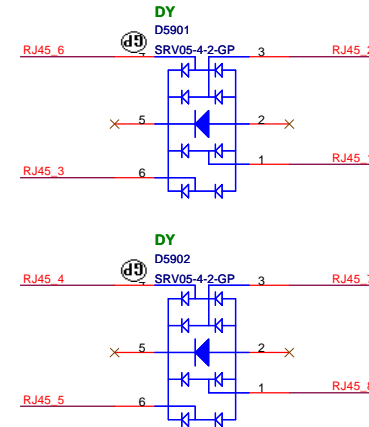
83.00005.BAE

DIODE ARR SRV05-4.TCT SOT-23-6

83.09904.AAE

DIODE ESD AZC099-04S SOT23-6L

Swap for V480



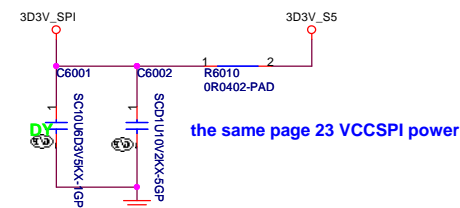
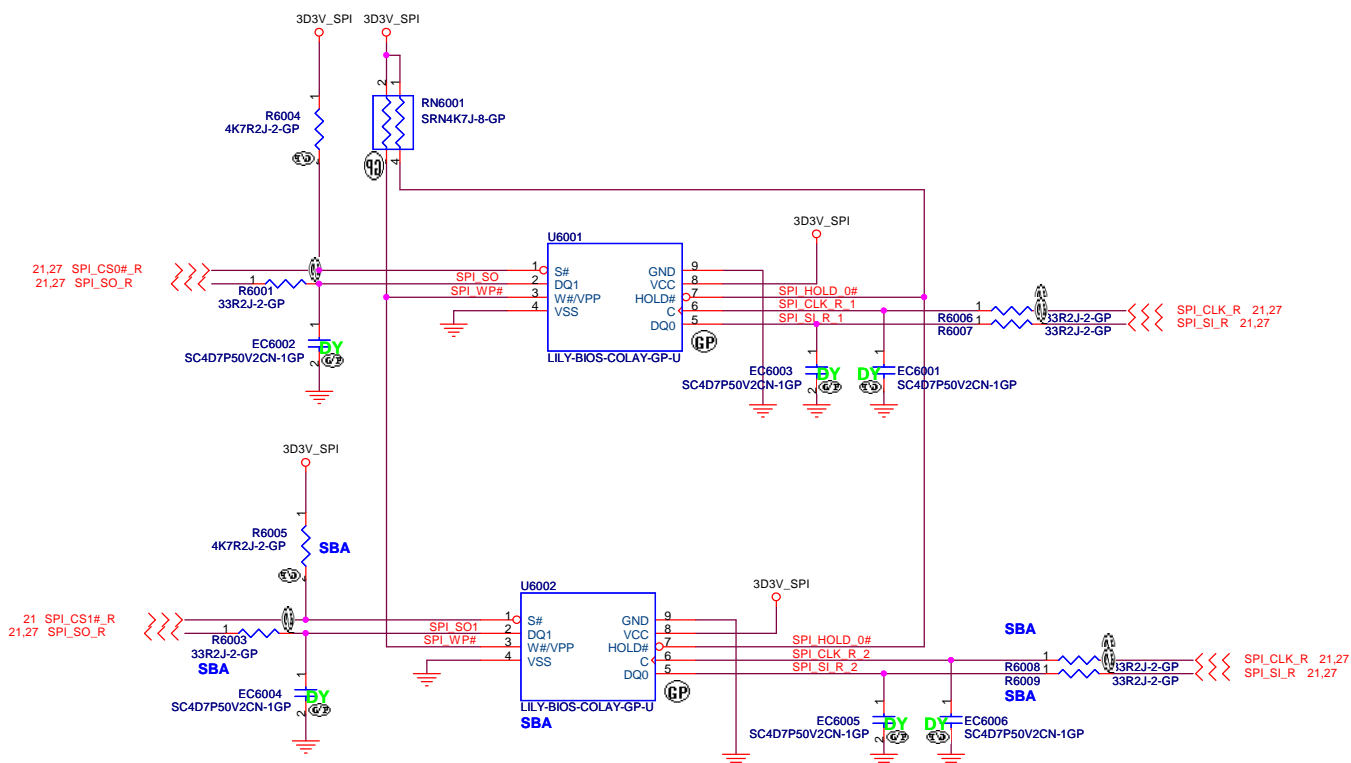
<Core Design>

緯創資通 Wistron Corporation
21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih,
Taipei Hsien 221, Taiwan, R.O.C.

Title		
RJ45 / Transformer		
Size	Document Number	Rev
A3	LA480	SD
Date:	Friday, January 06, 2012	Sheet 59 of 103

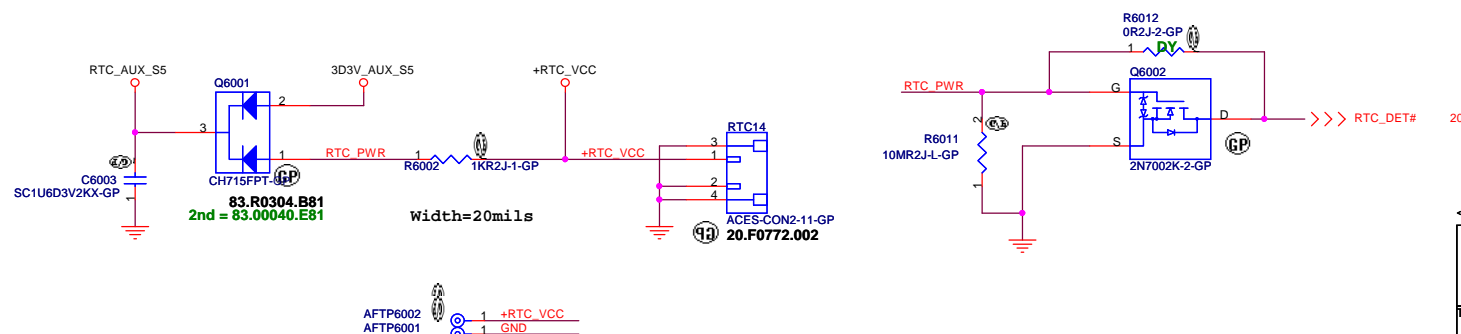
SSID = Flash.ROM

SPI FLASH ROM (8M byte) for PCH



4MB			
SO8	Marconix	MX25L3206EM2I-12G	72.25320.C01
	Winbond	W25Q032BVSSIG	72.25Q32.A01
	Numonyx	N25Q032A13ESE40	72.25032.H01
8MB			
SO8	Marconix	MX25L6406EM2I-12G	72.25640.D01
	Winbond	W25Q064CVSSIG	72.25Q64.B01
	Numonyx	N25Q064A13ESE40	72.25Q64.D01
16MB			
WSO8	Marconix	MX25L12836EZNI-10G	72.25128.X01
	Marconix	MX25L12835EZNI-10G	72.25128.Y01
	Winbond	W25Q128BVEIG	72.25128.I01
	Numonyx	N25Q128A13EF840	72.25128.B03

SSID = RBATT

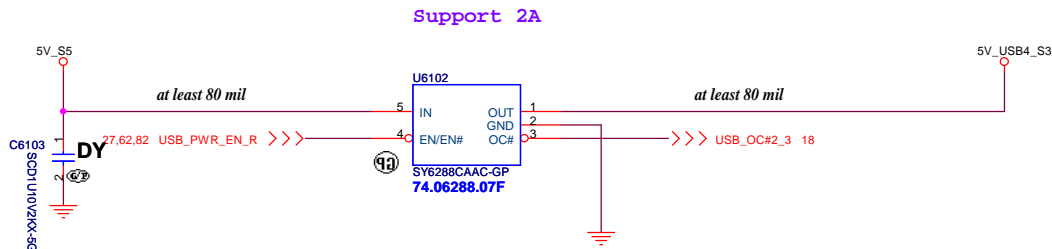


<Core Design>

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Taipei Hsien 221, Taiwan, R.O.C.

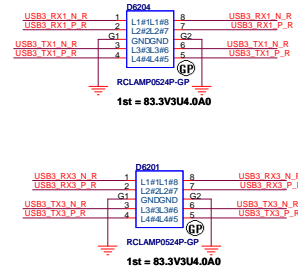
Title			Flash/RTC
Size	Document Number	Rev	SD
A3	LA480		
Date:	Friday, January 06, 2012	Sheet	60 of 103

USB Board CONN.



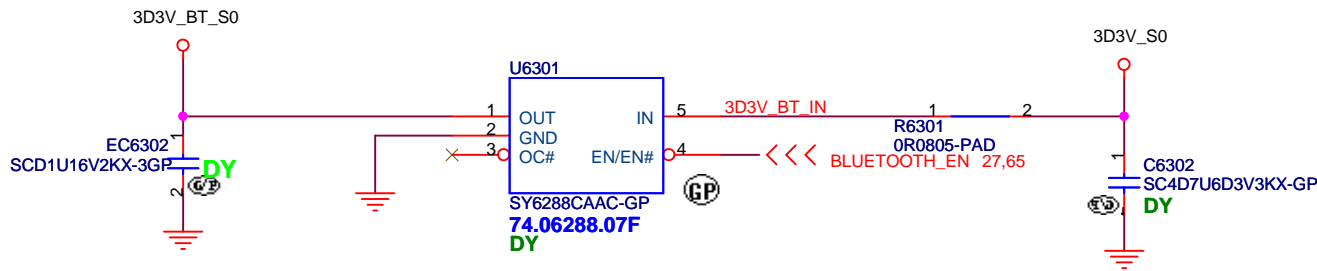
Place U6102 close to USBCN1

USB3.0 Port4



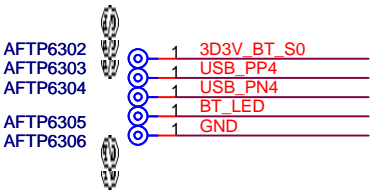
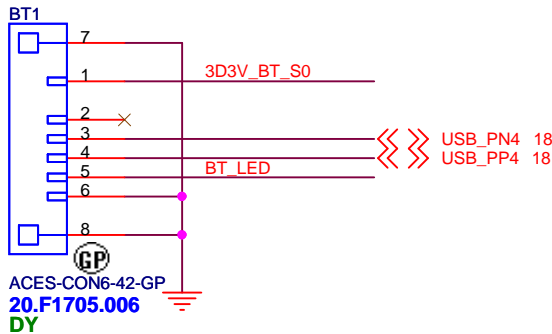
SSID = User.Interface

Bluetooth conn.



BT Module pin definition is same as LA470

SILERGY	74.06288.07F	SY6288CAAC	High Active
DIODES	74.02171.07F	AP2171WG-7	High Active
UPI	74.07534.A7F	OBS	High Active
GMT	74.05240.A7F	OBS	High Active



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Title

Bluetooth

Size

Document Number

Rev

A4

LA480

SD

Date

Friday, January 06, 2012

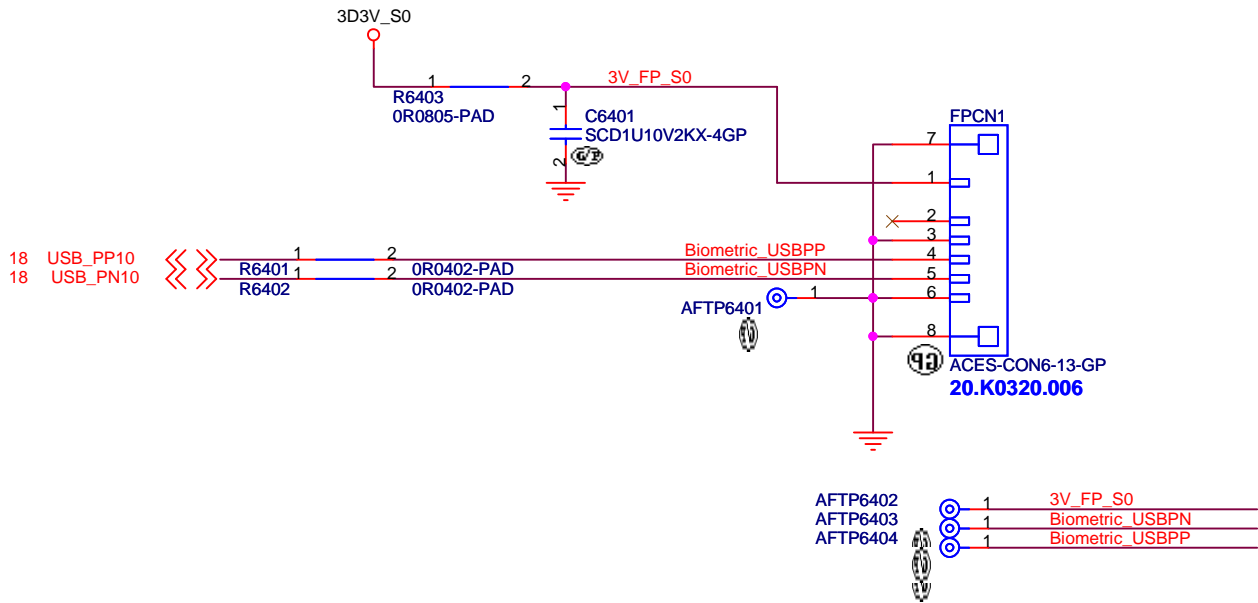
Sheet

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of

103

Finger Printer Connector

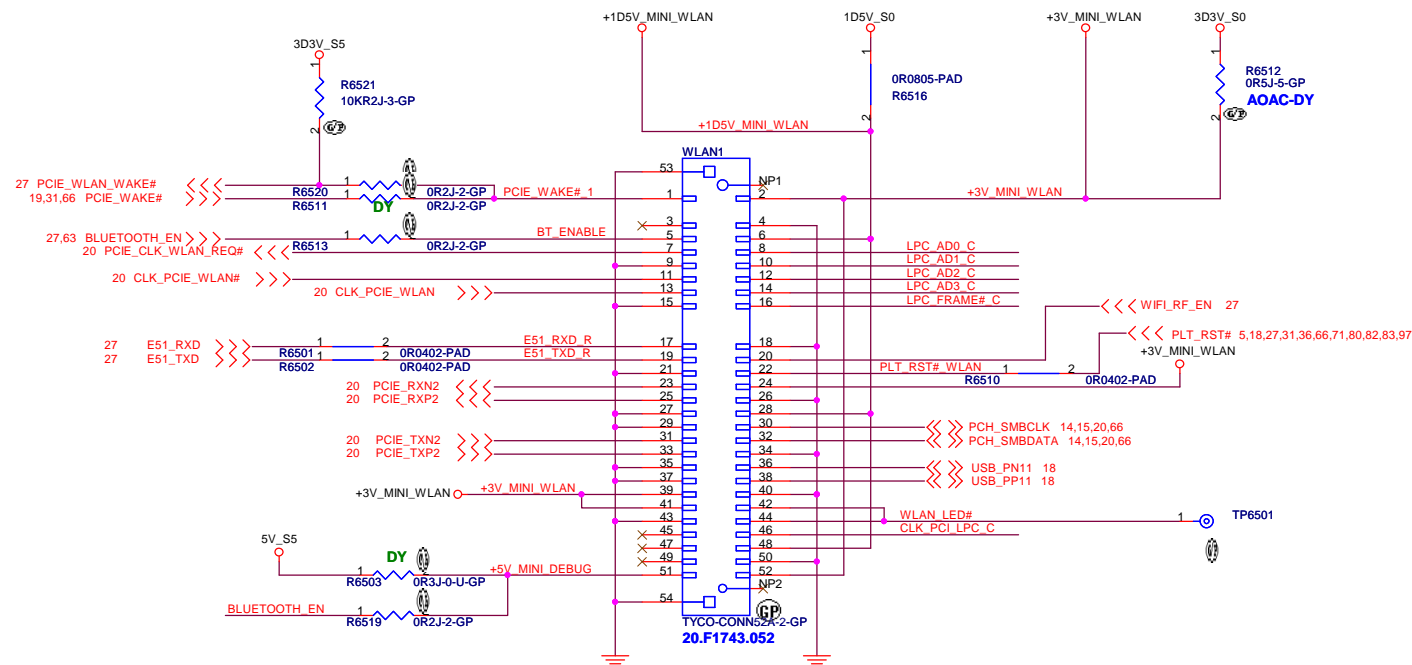


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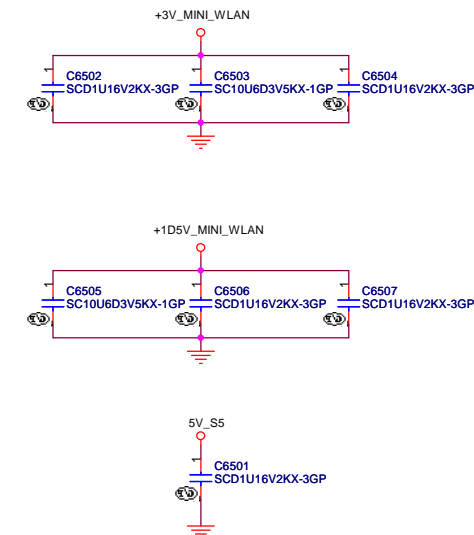
緯創資通		Wistron Corporation	
		21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title			
Finger Printer Connector			
Size A4	Document Number LA480		Rev SD
Date:	Friday, January 06, 2012	Sheet 64 of	103

SSID = Wireless

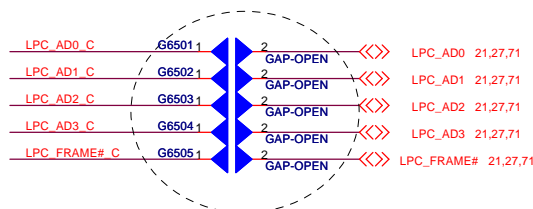
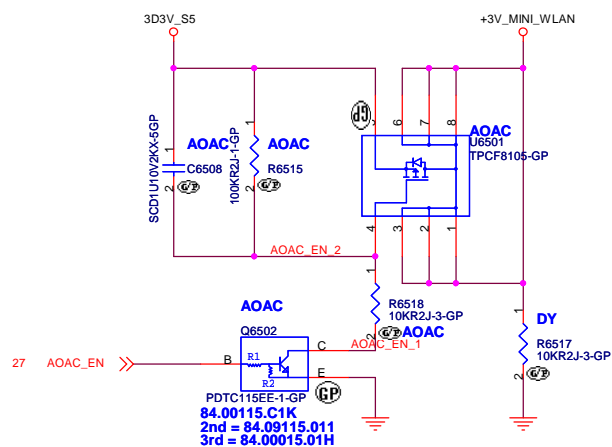
Mini Card Connector(802.11a/b/g/n)



Place near MINI Card CONN



Reserve for AOAC



G6506~G6511
placement close close WLAN1
in bottom side

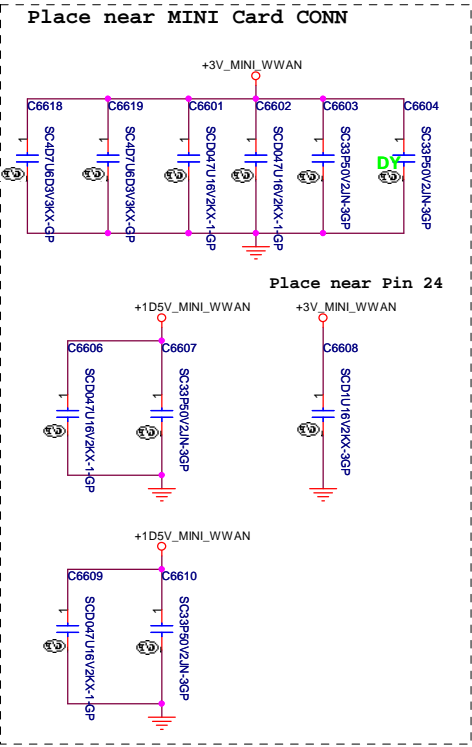
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緯創資通 Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

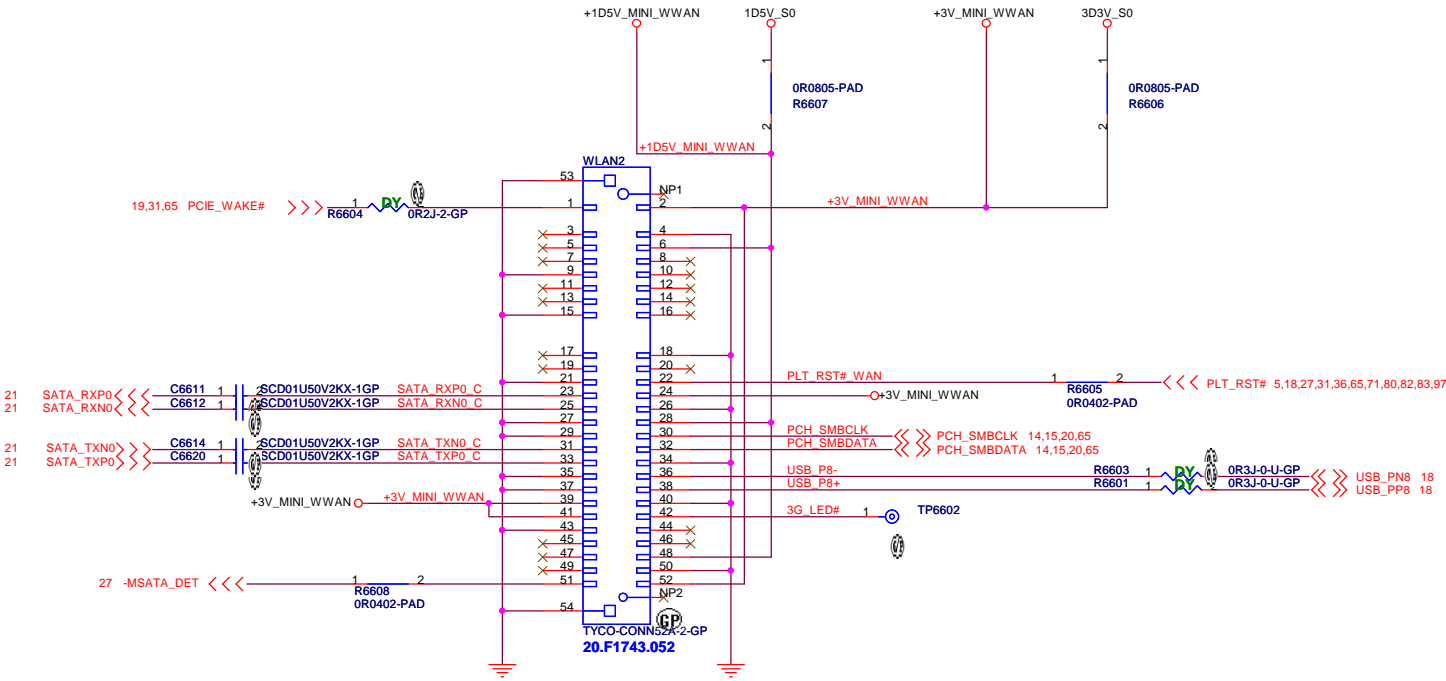
Title: MINICARD(WLAN)/TP CONN
Size A3 Document Number: LA480 Rev SD
Date: Friday, January 06, 2012 Sheet 65 of 103

SSID = Wireless

mSATA for V Series Only



Mini Card Connector(Full Card)



<Core Design>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

WWAN Connector

Size
A3

Document Number

LA480

Rev
S

Date: Friday, January 06, 2012

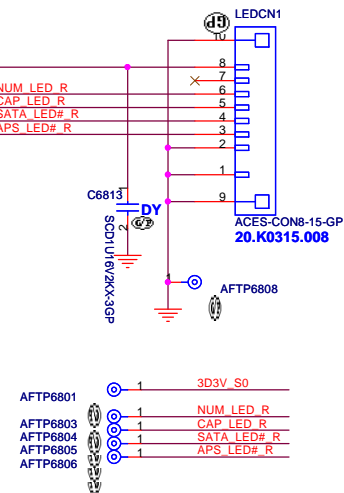
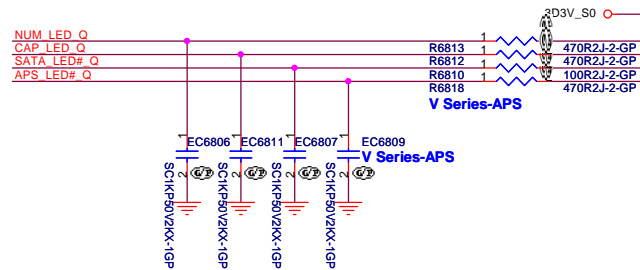
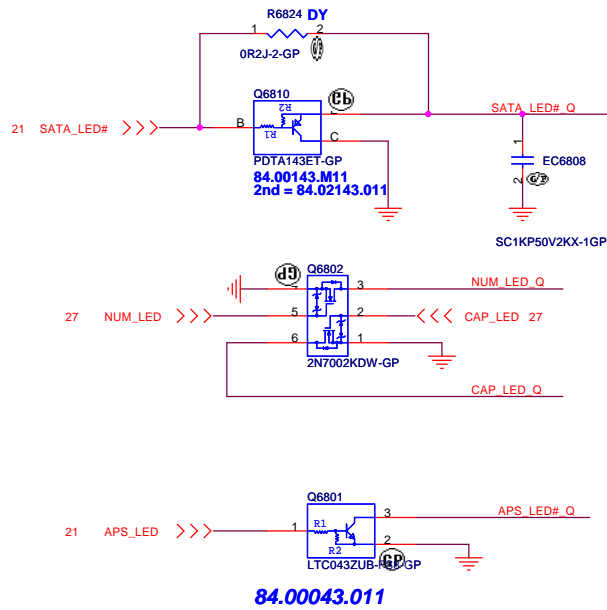
Sheet 66 of 103

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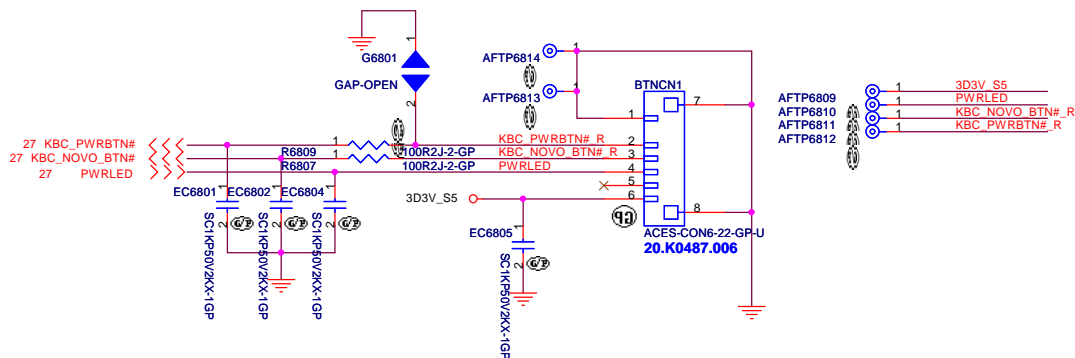
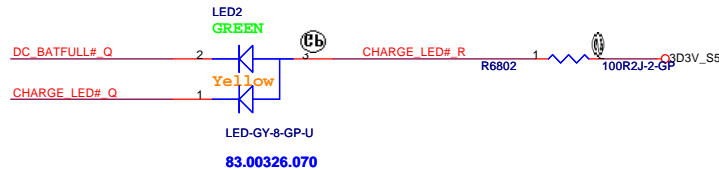
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Title Reserved			
Size A4	Document Number LA480		Rev SD
Date: Friday, January 06, 2012		Sheet 67 of	103

SSID = User.Interface



CHARGER LED

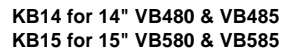


<Core Design>

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Title		
LED Bard/Power Button		
Size	Document Number	Rev
A3	LA480	SD
Date:	Friday, January 06, 2012	Sheet 68 of 103

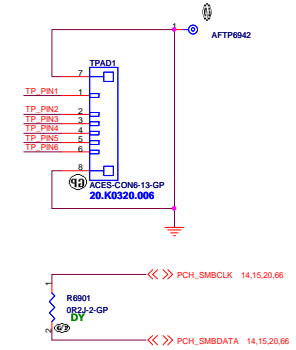
Internal KeyBoard Connector



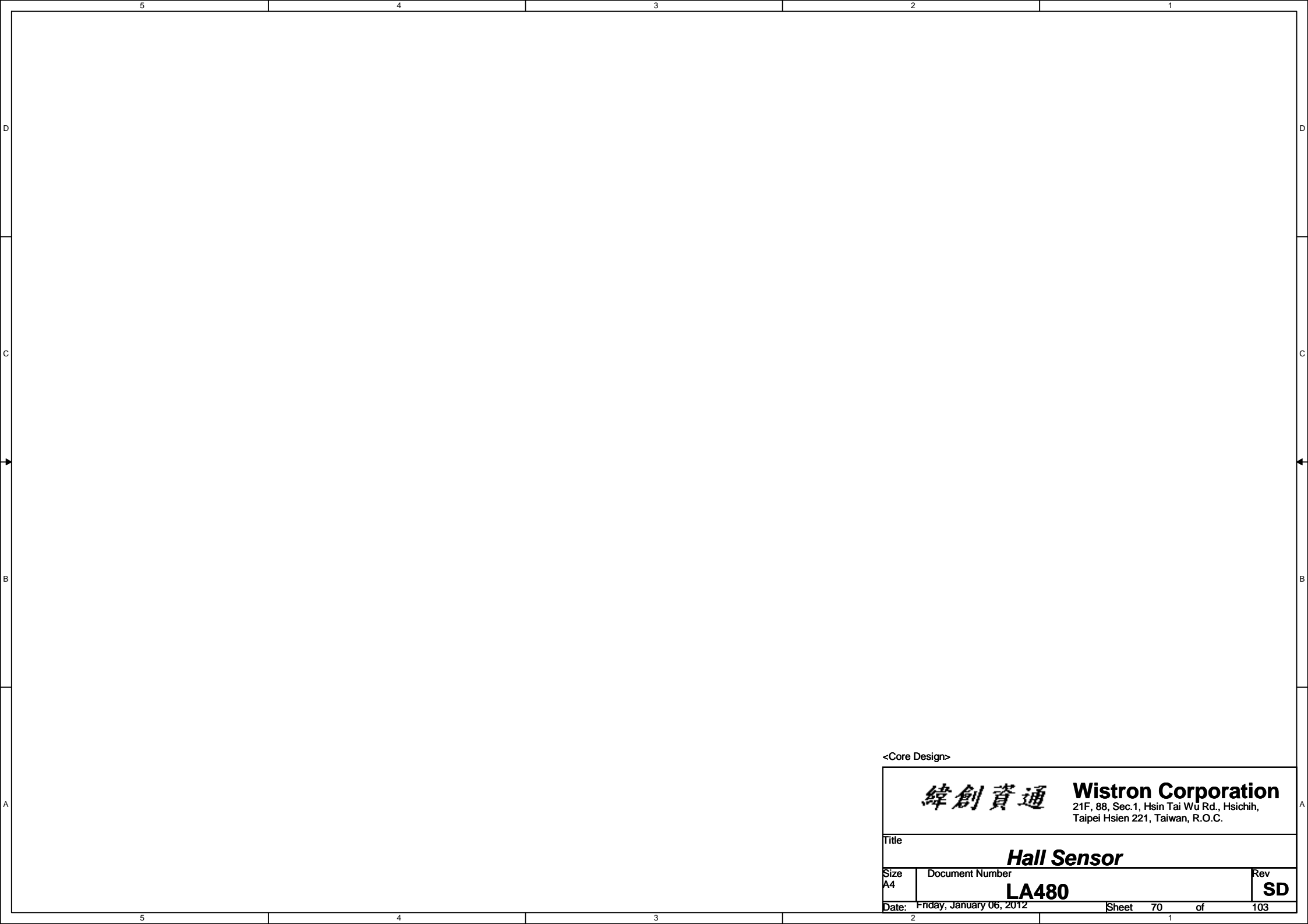
PIN #	7	11	13	18	14	10	17	15	16	4	23	22	19	20	21	24	12	1	8	9	5	6	3	2
As-sign	D 1	D 2	D 3	D 4	D 5	D 6	D 7	D 8	D 9	D 10	D 11	D 12	D 13	D 14	D 15	D 16	S 1	S 2	S 3	S 4	S 5	S 6	S 7	S 8

[illegible]

The schematic diagram illustrates the electrical connections for the B Series-TP and V Series-TP. It shows two main signal paths. The top path, labeled 'B Series-TP', starts with a red 'TP SW_L' signal connected to a red 'TP SW_R' signal through a resistor 'R6903'. This is followed by a 19 ohm resistor, then a red 'TP DATA' signal connected to a red 'TP PNE' signal through a resistor 'R6904'. The bottom path, labeled 'V Series-TP', starts with a blue 'TP CLK' signal connected to a blue 'TP PNI' signal through a resistor 'R6906'. This is followed by a 19 ohm resistor, then a red 'TP DATA' signal connected to a red 'TP PNI' signal through a resistor 'R6907'. Both paths are connected to a 5V_S0 signal (blue) and a 303V_S0 signal (blue). The B Series-TP path also includes a C6901 capacitor, and the V Series-TP path includes a C6902 capacitor.



	Models			
Synaptics PIN	B480	V480	B580	V580
TM-01146-006	✓			
TM-02123-001		✓		
TM-02060-001			✓	
TM-02045-001				✓
VDD	5V	3.3V	5V	3.3V
Pin 1	VDD	VDD	VDD	VDD
Pin 2	CLK	CLK	CLK	CLK
Pin 3	DA7	DA7	DA7	DA7
Pin 4	Left button	GND	Right button	GND
Pin 5	Right button	NC	Left button	NC
Pin 6	GND	NC	Right button	NC



<Core Design>

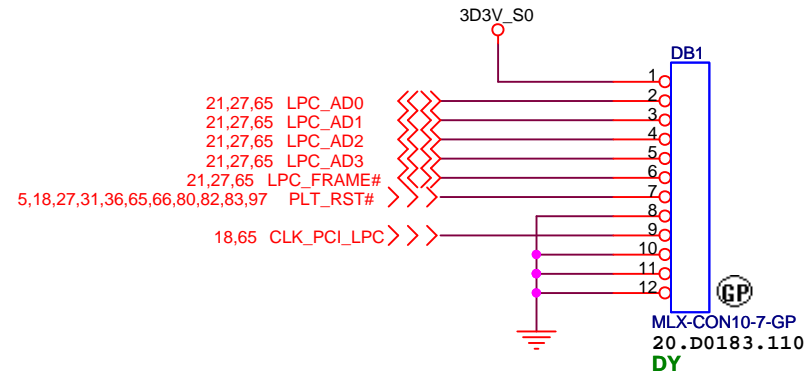
緯創資通

Wistron Corporation
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Taipei Hsien 221, Taiwan, R.O.C.

Title

Hall Sensor

Size A4	Document Number LA480	Rev SD
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<Core Design>

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Title

Dubug connector

Size
A4

Document Number

LA480

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SD

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<Core Design>

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Title Reserved			
Size A4	Document Number LA480		Rev SD
Date: Friday, January 06, 2012		Sheet 72 of	103

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<Core Design>

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Title Reserved			
Size A4	Document Number LA480		Rev SD
Date: Friday, January 06, 2012		Sheet 73 of	103



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緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

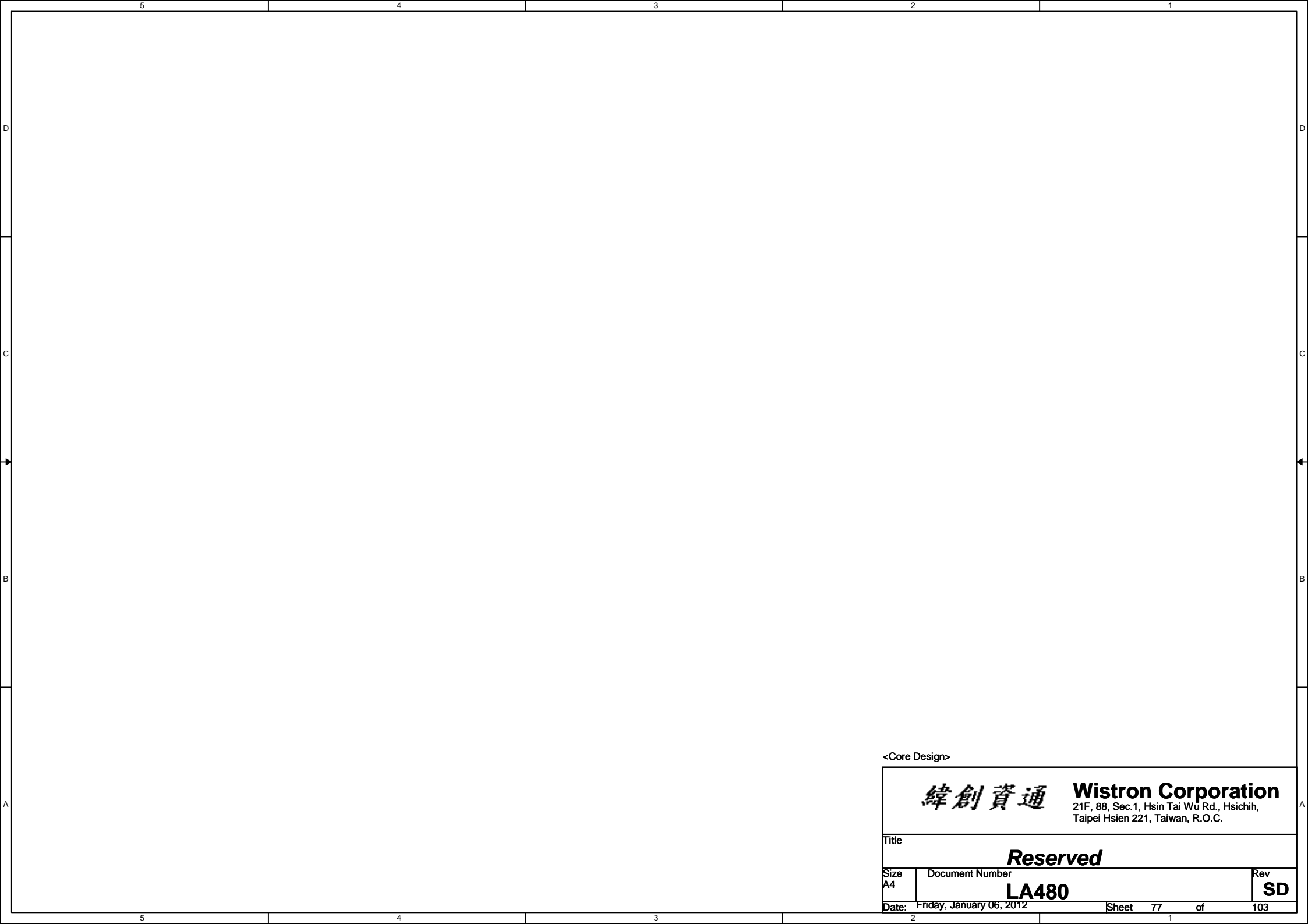
New Card

Size A4	Document Number LA480	Rev SD
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<Core Design>

		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Reserved			
Size A4	Document Number LA480		Rev SD
Date: Friday, January 06, 2012		Sheet 76 of	103



<Core Design>

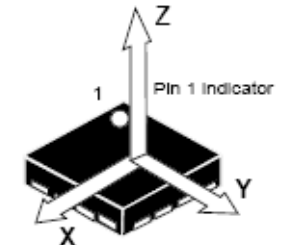
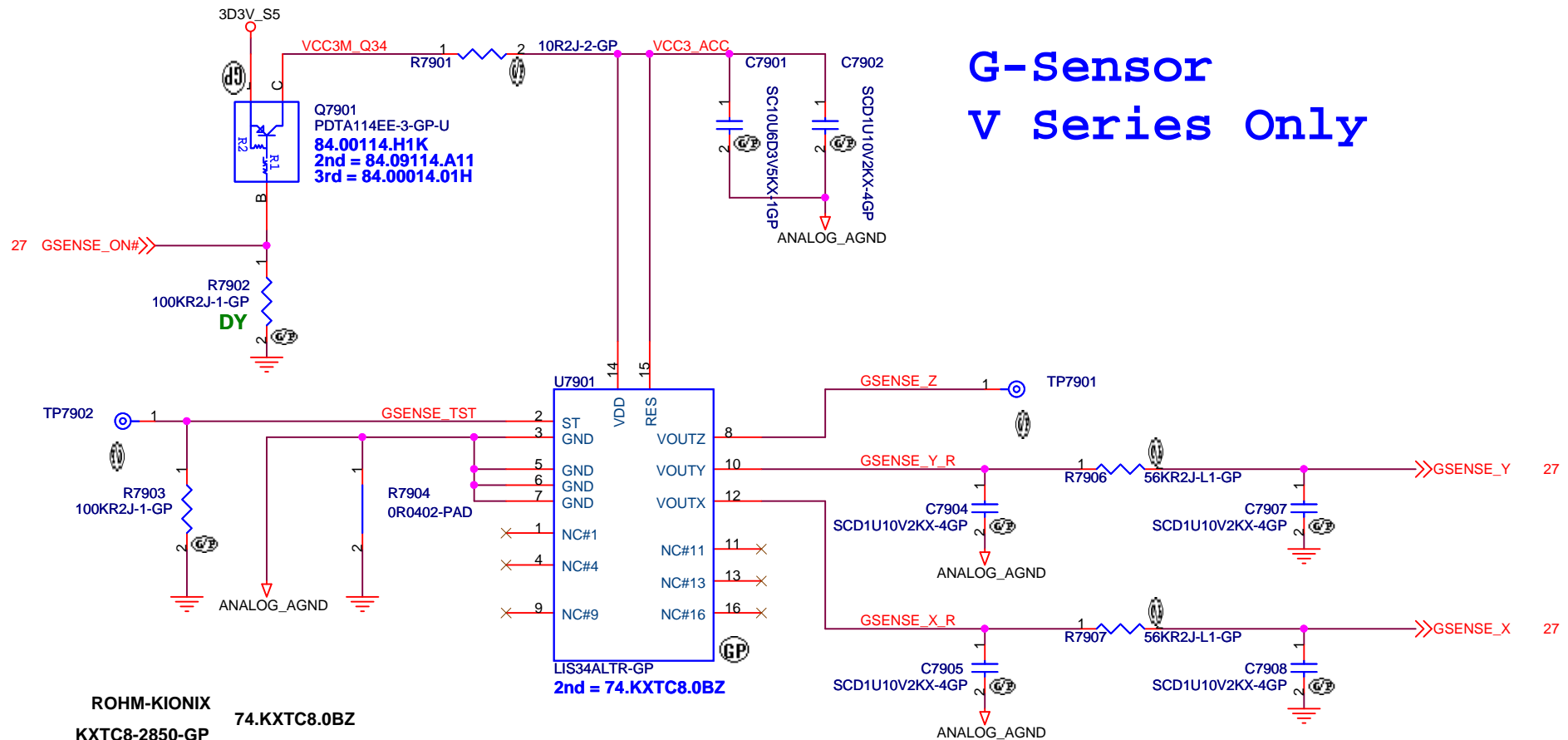
		Wistron Corporation 21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.	
Title Reserved			
Size A4	Document Number LA480		Rev SD
Date: Friday, January 06, 2012		Sheet 77 of	103

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<Core Design>

<div>緯創資通</div>		<div>Wistron Corporation</div>	
		<div>21F, 88, Sec.1, Hsin Tai Wu Rd., Hsichih, Taipei Hsien 221, Taiwan, R.O.C.</div>	
<div>Title</div>			
<div>Reserved</div>			
<div>Size</div>	<div>Document Number</div>		<div>Rev</div>
<div>A4</div>	<div>LA480</div>		<div>SD</div>
<div>Date: Friday, January 06, 2012</div>		<div>Sheet 78 of</div>	<div>103</div>

G-Sensor V Series Only



Layout Comment :

- (1) Place C483, C484, Q46, R528, R530, C479, C476, R509, R508 close to U55.
- (2) Avoid routing under DCDC switching area.

<Core Design>

緯創資通

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Title

G-Sensor

Size
A4

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LA480

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SD

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RFID

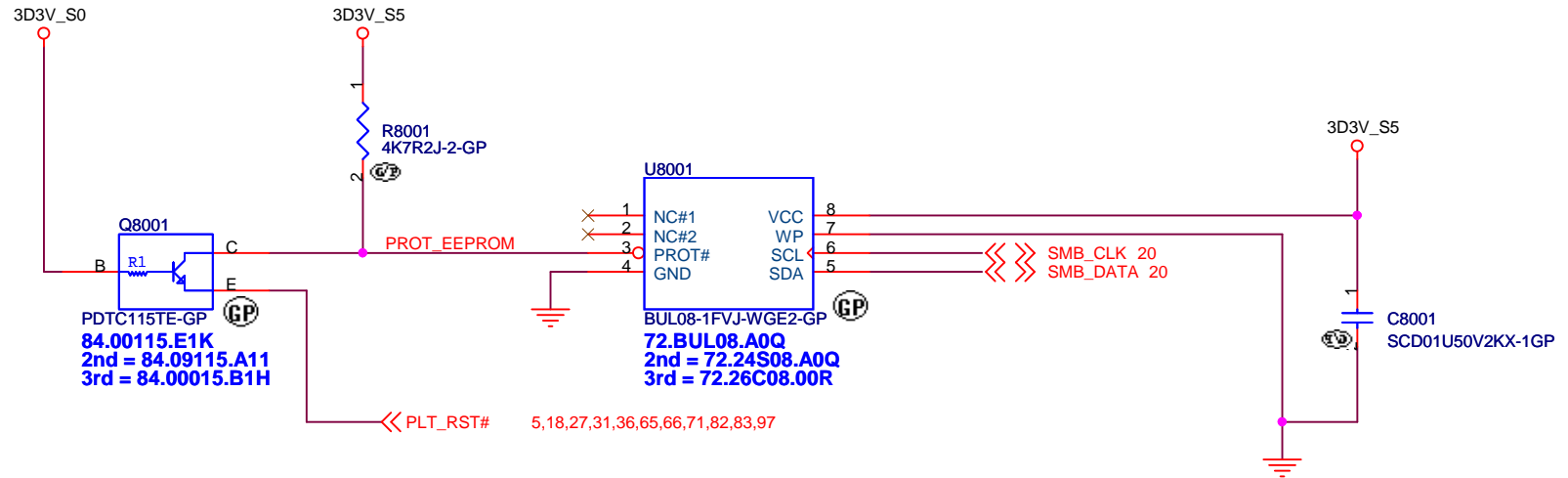



Table 80.1- Transistor multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
NXP	PDT115TE	N/A	84.00115.E1K
ROHM	LTC015TEB	N/A	84.00015.B1H
Panasonic	DRC9115T0L	N/A	84.09115.A11

Table 80.2- EEPROM multi-source

Supplier	Description	Lenovo P/N	Wistron P/N
ROHM	BUL08-1FVJ-WGE2	N/A	72.BUL08.A0Q
NXP	PCA24S08ADP	N/A	72.24S08.A0Q
SANYO	LE26CAP08TT-TLM-H	N/A	72.26C08.00R

<Core Design>

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Title	
RF ID	
Size A4	Document Number LA480
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<Core Design>

緯創資通

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Taipei Hsien 221, Taiwan, R.O.C.

Title

Reserved

Size
A4

Document Number

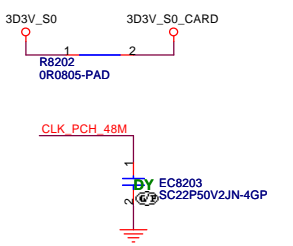
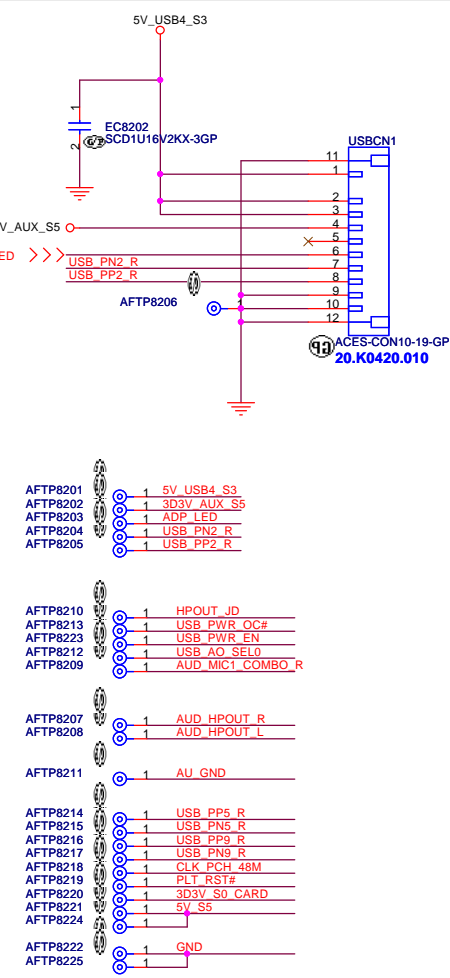
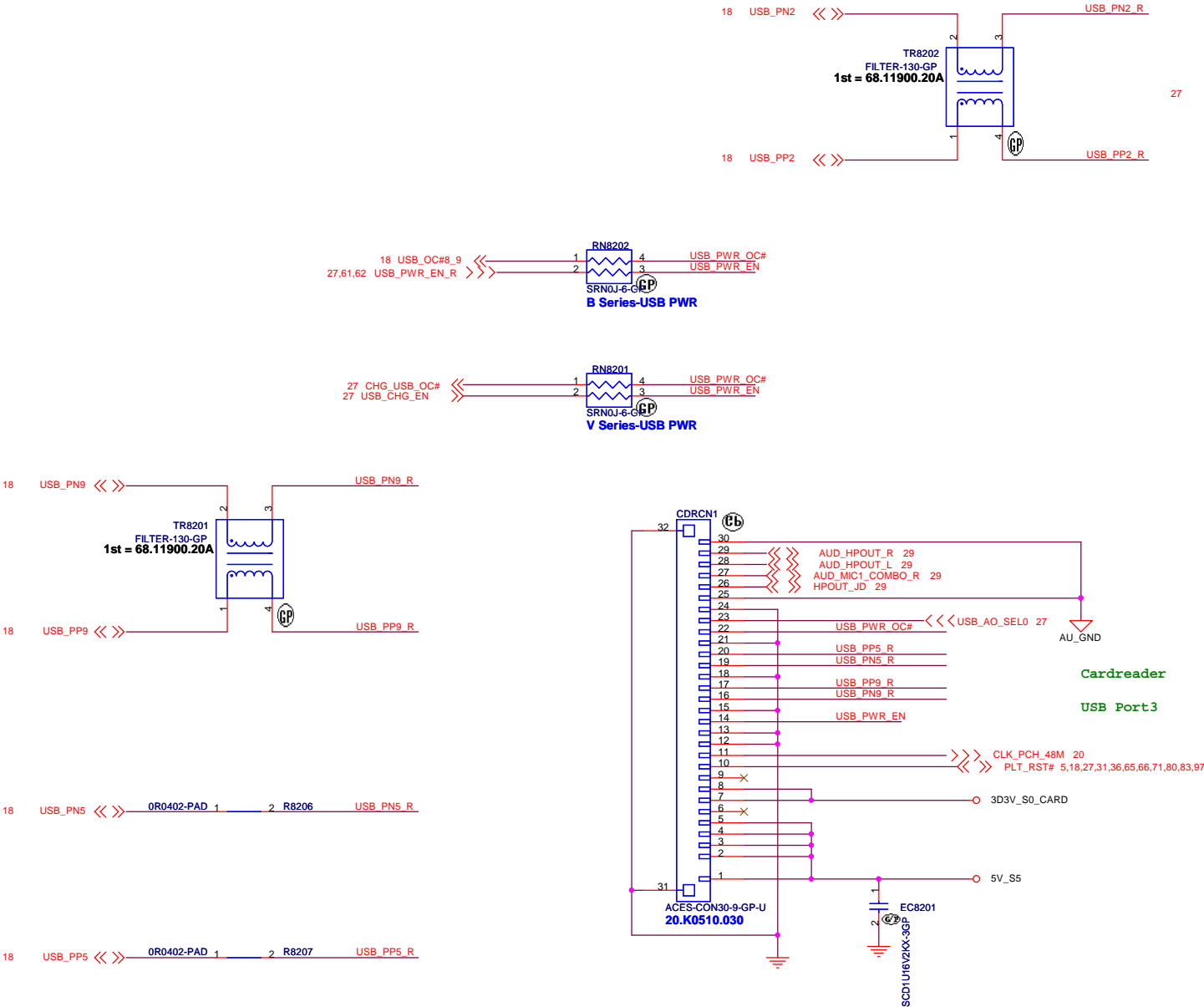
LA480

Rev
SD

Date: Friday, January 06, 2012

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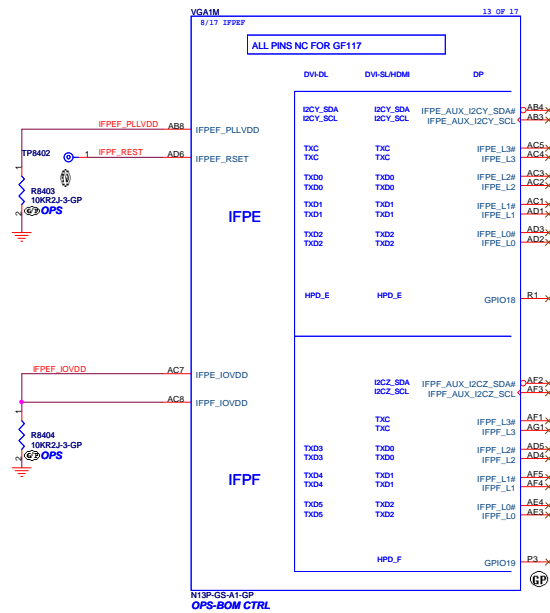
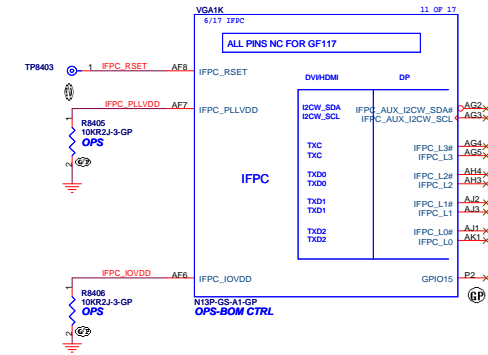
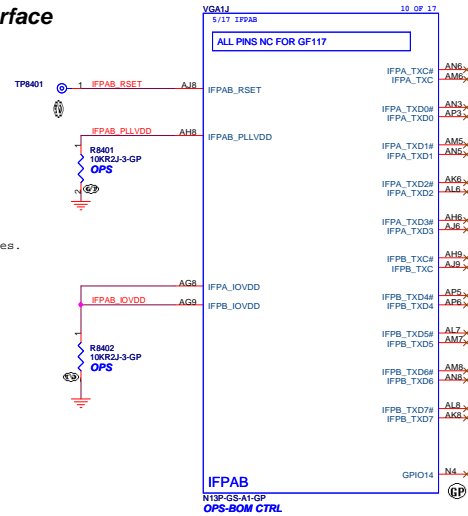
R8201 and R8203 Dual layout with TR8201



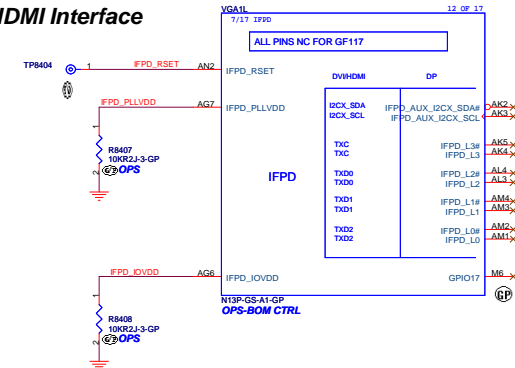


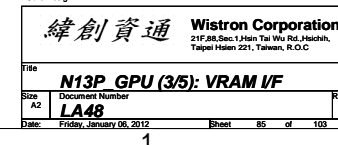
LVDS Interface

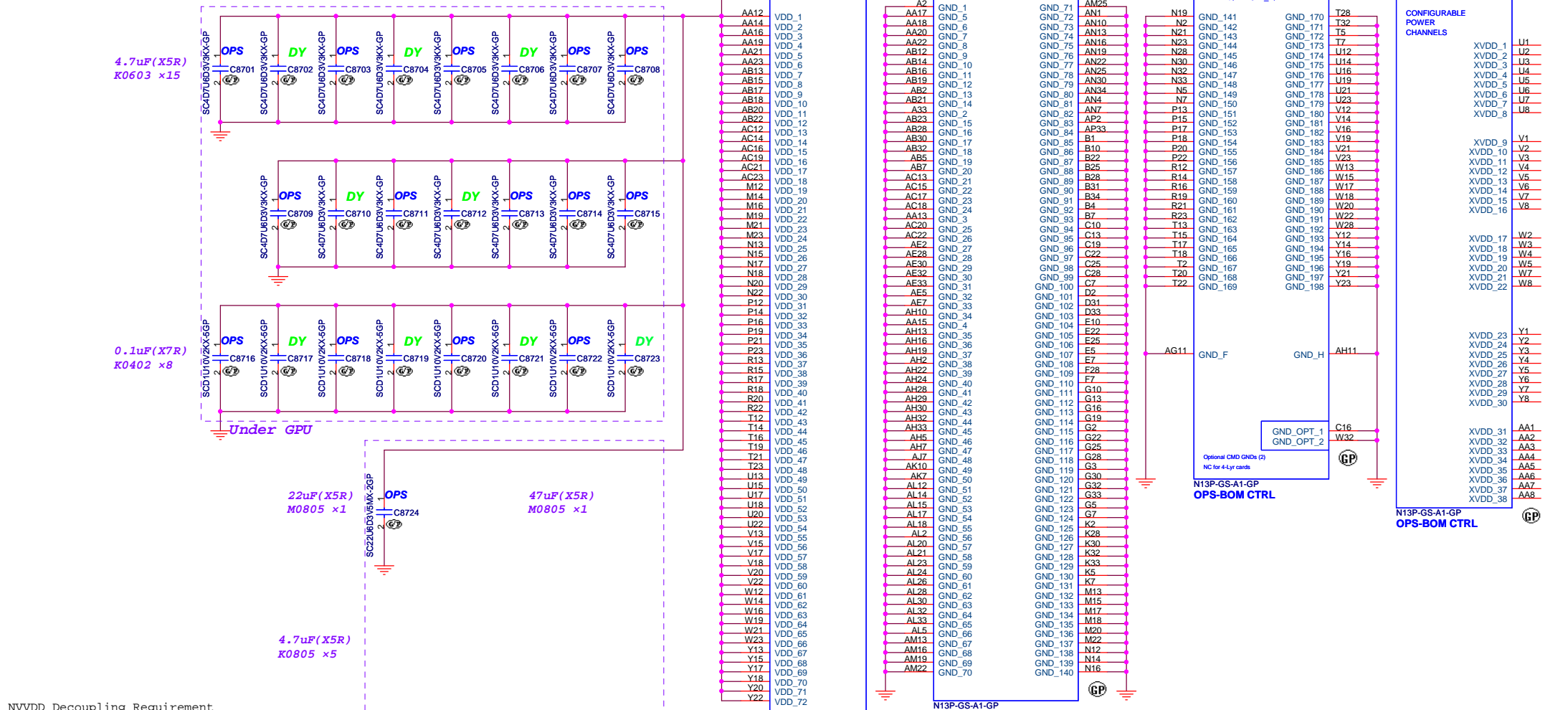
SPEC. (DG-05587-001_v03_p.160)
Pull down IFPxy IOVDD with 10kΩ resistor.
Pull down IFPxy PLLVDD with 10kΩ resistor.
The other IO pins can be NC, this includes unused data lines.



HDMI Interface







NVDD Decoupling Requirement
(DG-05587-001_v03_p.56_Table 7)

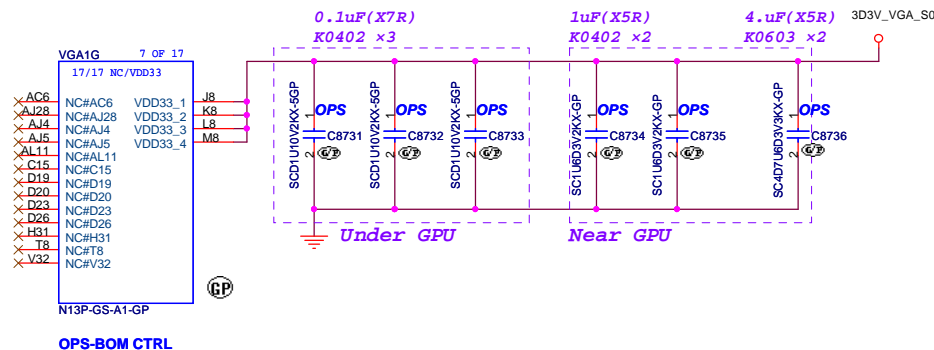
Capacitor Type	Footprint	Population	Location
4.7uF	X6S	0603	15
0.1uF	X7R	0402	8
47uF	X5R	0805	1
22uF	X5R	0805	1
4.7uF	X5R	0805	5

X7R (+/-15%、-55~125℃)
X6S (+/-22%、-55~105℃)
X5R (+/-15%、-55~85℃)

VDD33 Decoupling (DG-05587-001_v03_p.57_Table 8)

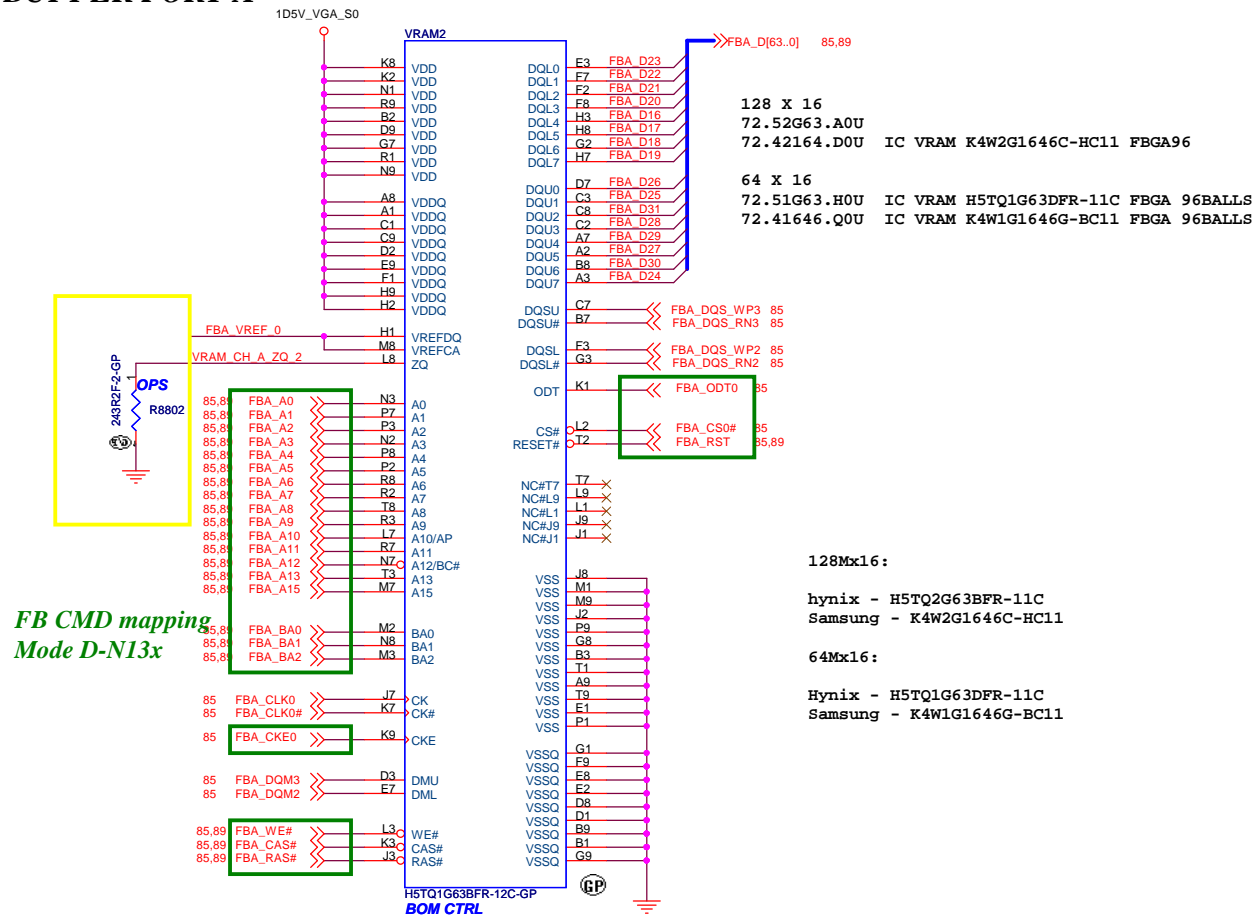
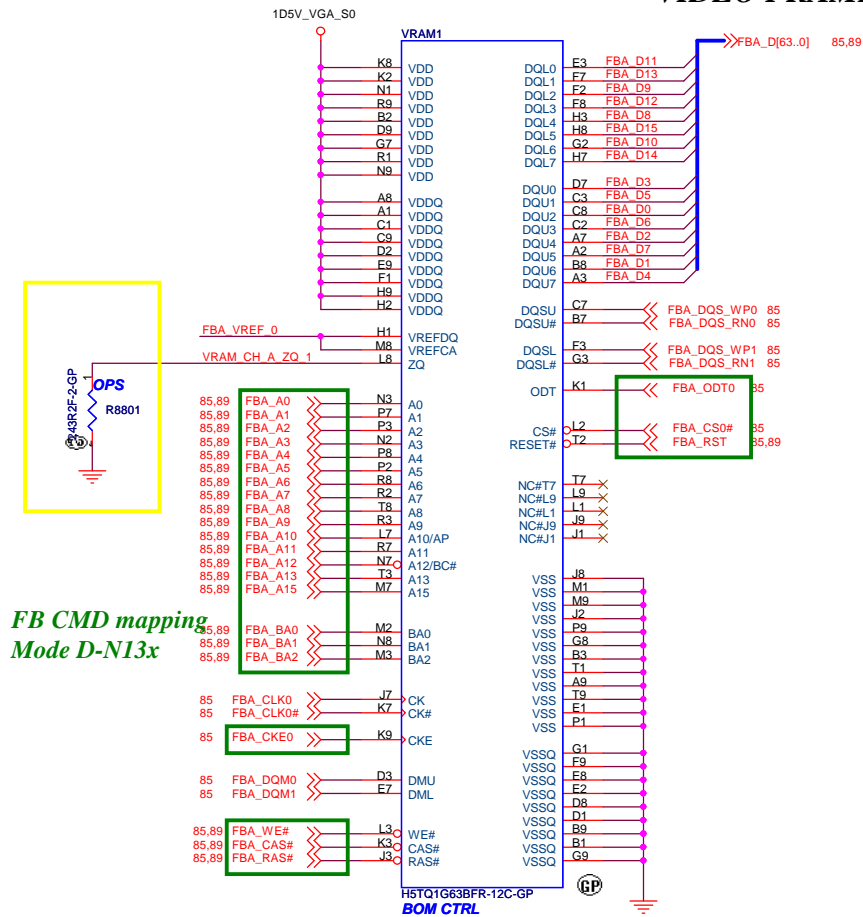
Capacitor Type	Footprint	Population	Location
0.1uF	X7R	0402	3
1uF	X5R	0402	2
4.7uF	X5R	0603	1

X7R (+/-15%、-55~125℃)
X5R (+/-15%、-55~85℃)



<Core Design>

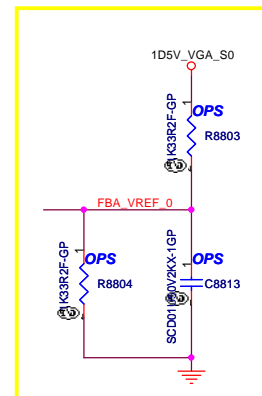
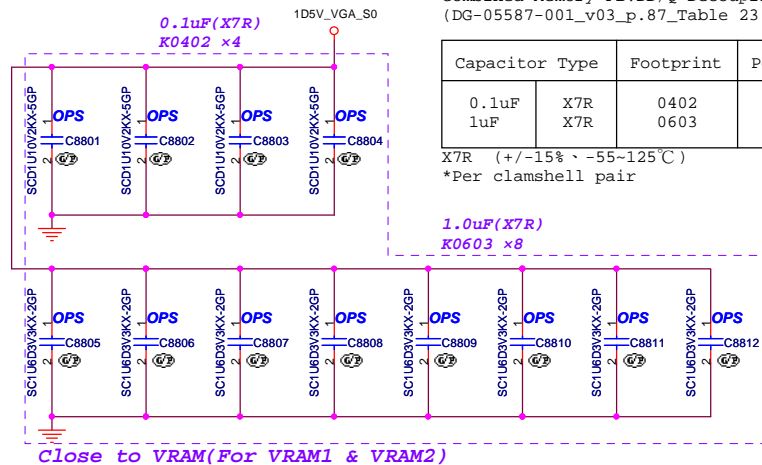
VIDEO FRAME BUFFER PORT A



Combined Memory FBVDD/Q Decoupling DDR3x16 with Clamshell Layout
(DG-05587-001_v03_p.87_Table 23)

Capacitor Type		Footprint	Population	Location
0.1uF	X7R	0402	4	Close to VRAM
1uF	X7R	0603	8	Close to VRAM

X7R (+/-15%、-55~125°C)
*Per clamshell pair



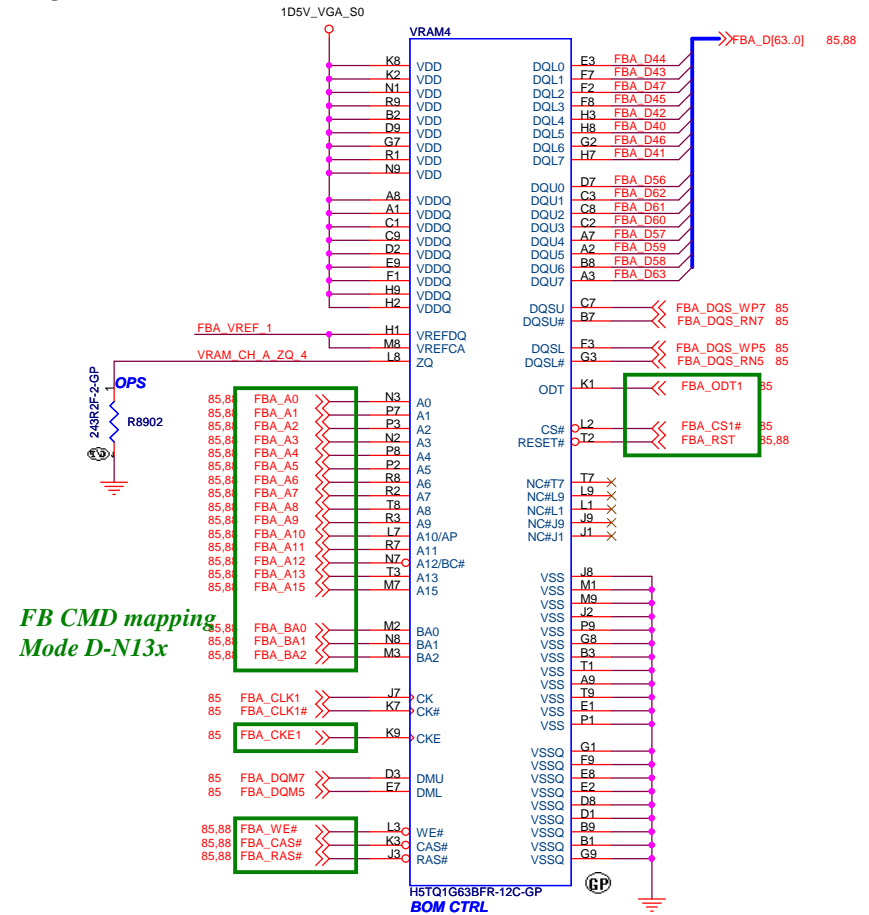
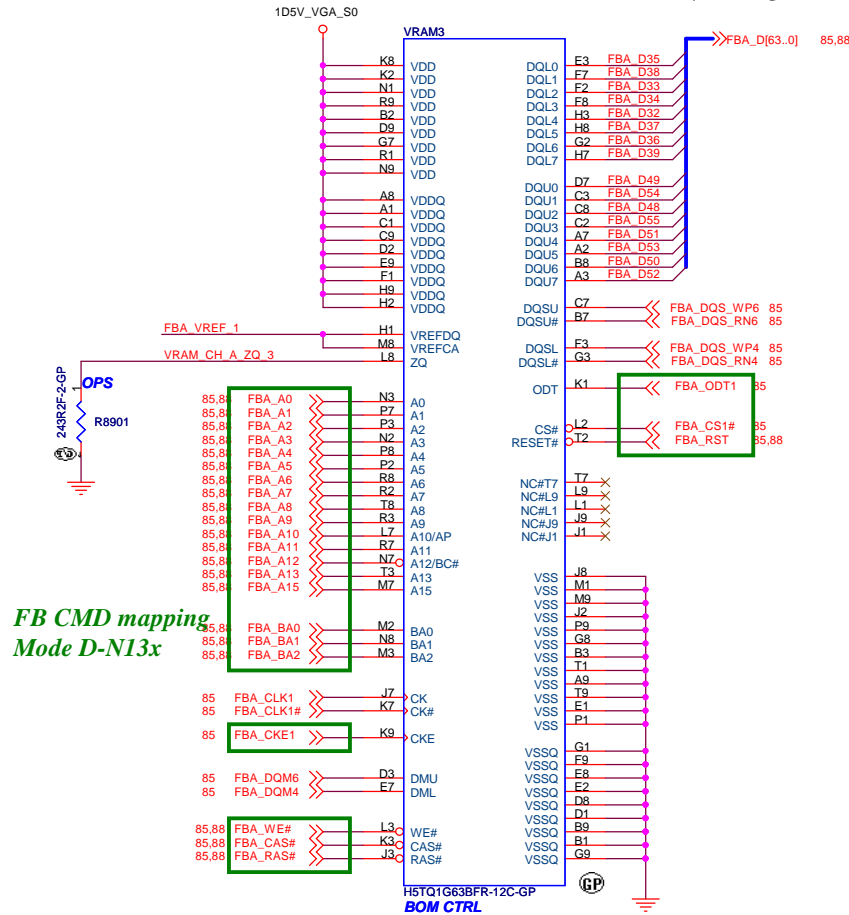
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Title	CHANNEL-A_VRAM1,2 (1/4)
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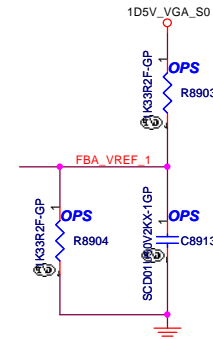
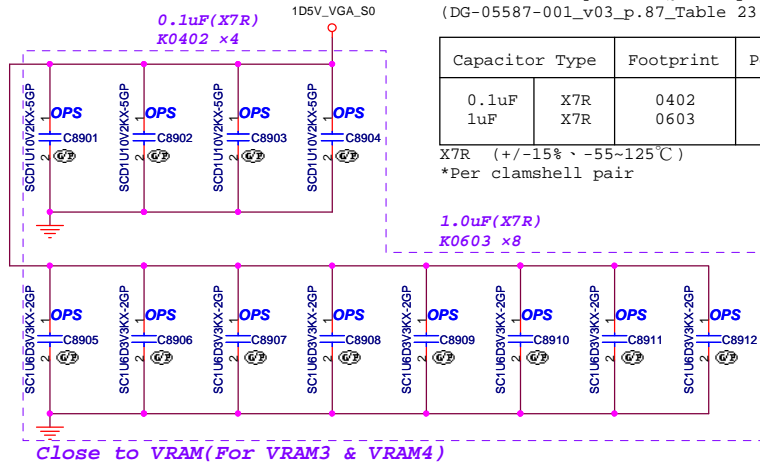
VIDEO FRAME BUFFER PORT A



Combined Memory FBVDD/Q Decoupling DDR3x16 with Clamshell Layout (DG-05587-001_v03_p.87_Table 23)

Capacitor Type	Footprint	Population	Location
0.1uF	X7R	0402	4
1uF	X7R	0603	8

X7R (+/-15%、-55-125°C)
*Per clamshell pair

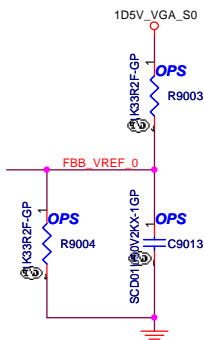
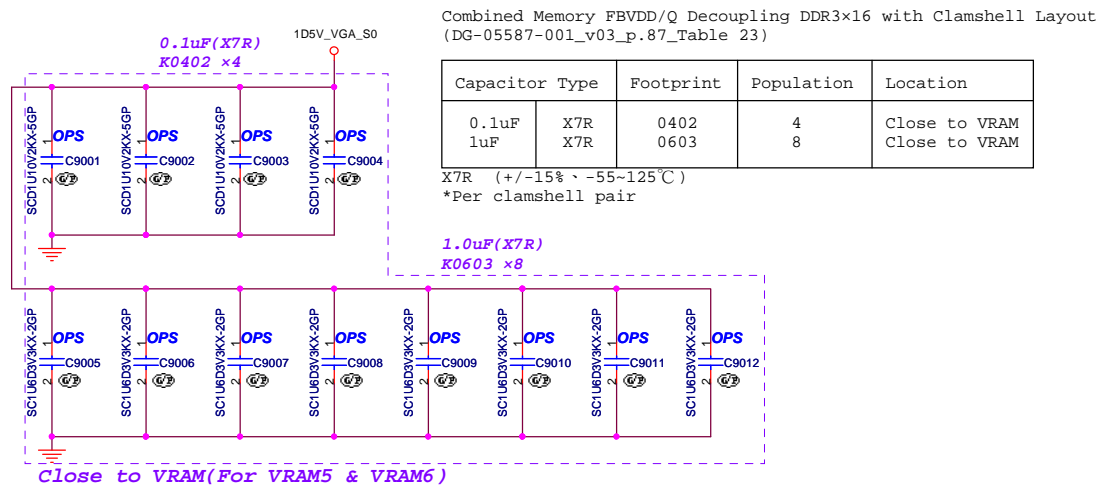
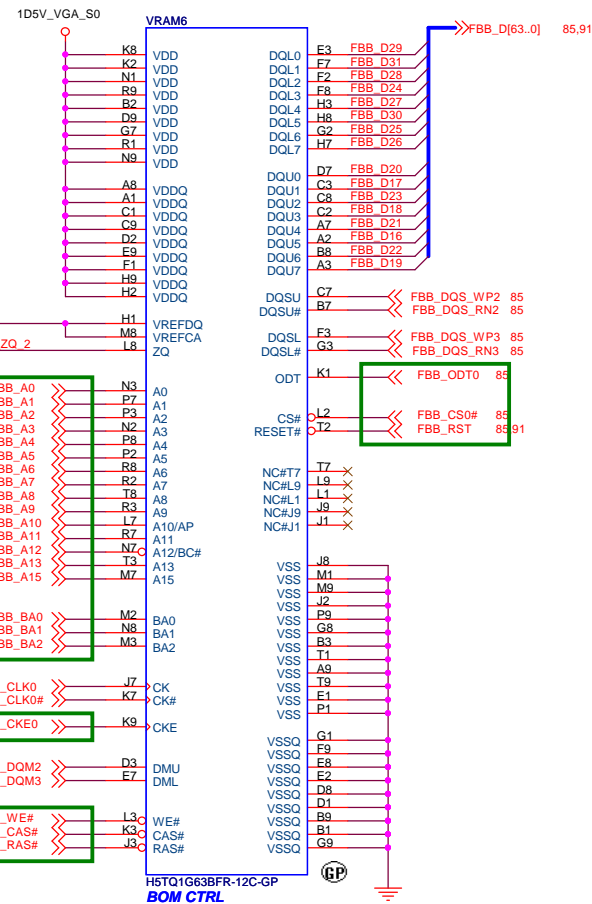
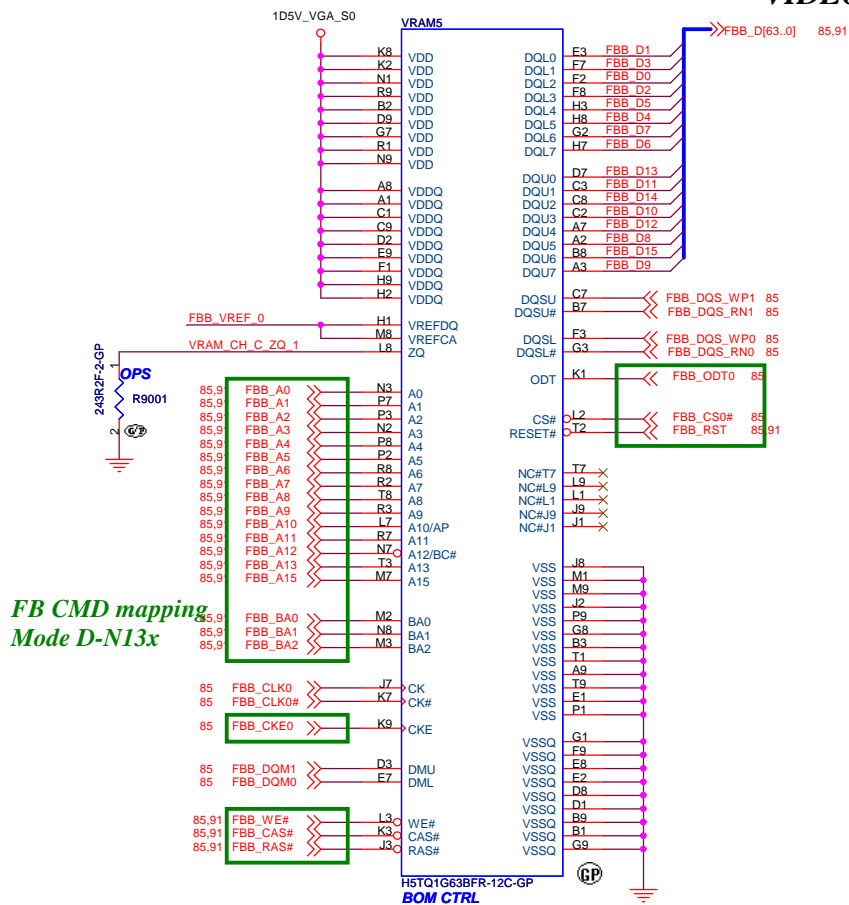


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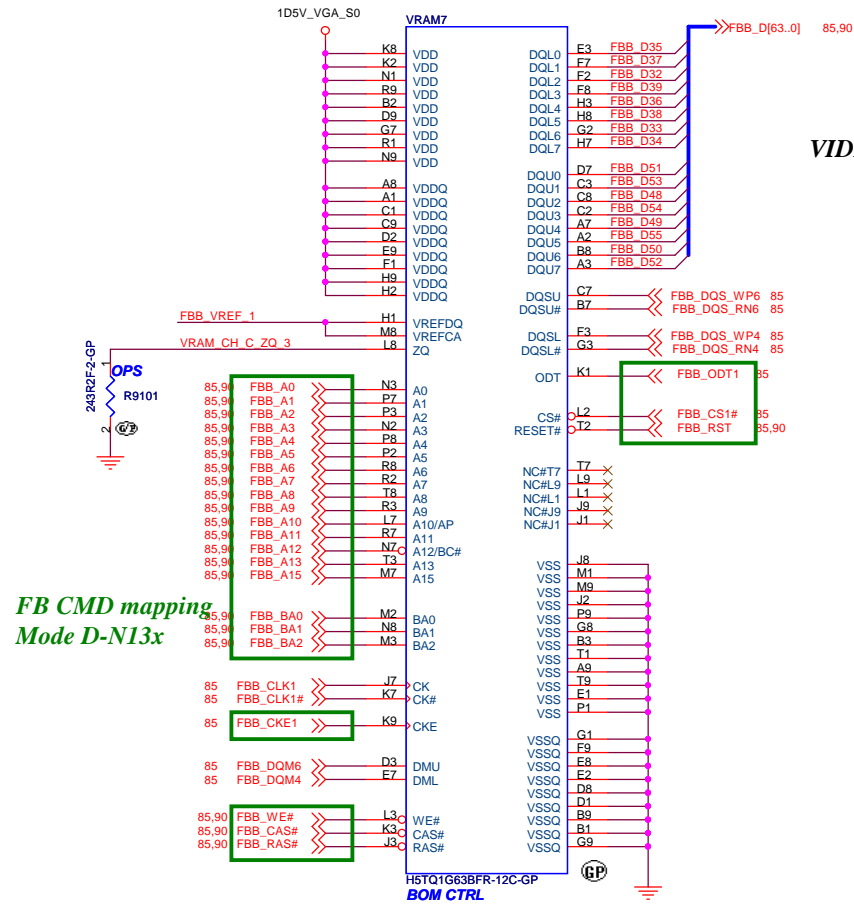
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Title	CHANNEL-A_VRAM3,4 (2/4)		
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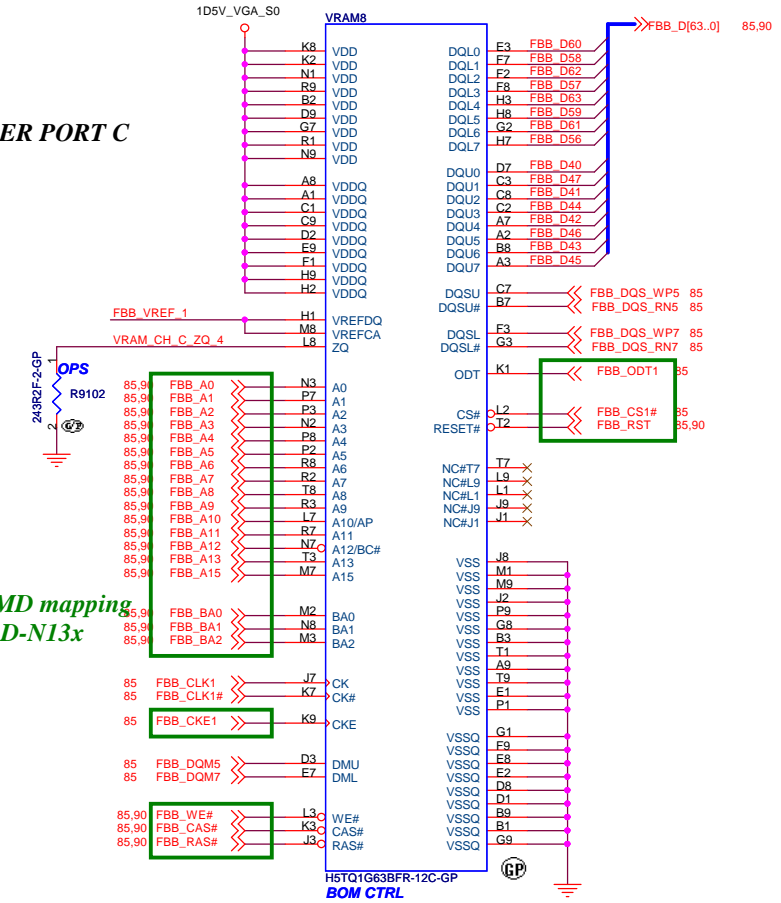
VIDEO FRAME BUFFER PORT C



VIDEO FRAME BUFFER PORT C



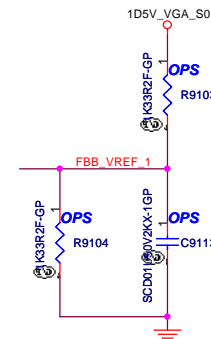
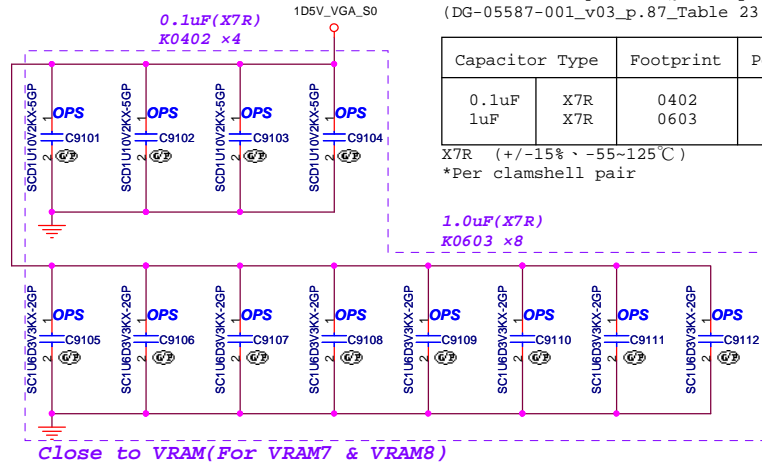
FB CMD mapping Mode D-N13x



Combined Memory FBVDD/Q Decoupling DDR3×16 with Clamshell Layout (DG-05587-001_v03_p.87_Table 23)

Capacitor Type	Footprint	Population	Location
0.1uF	X7R	0402	4
1uF	X7R	0603	8

X7R (+/-15%、-55-125°C)
*Per clamshell pair



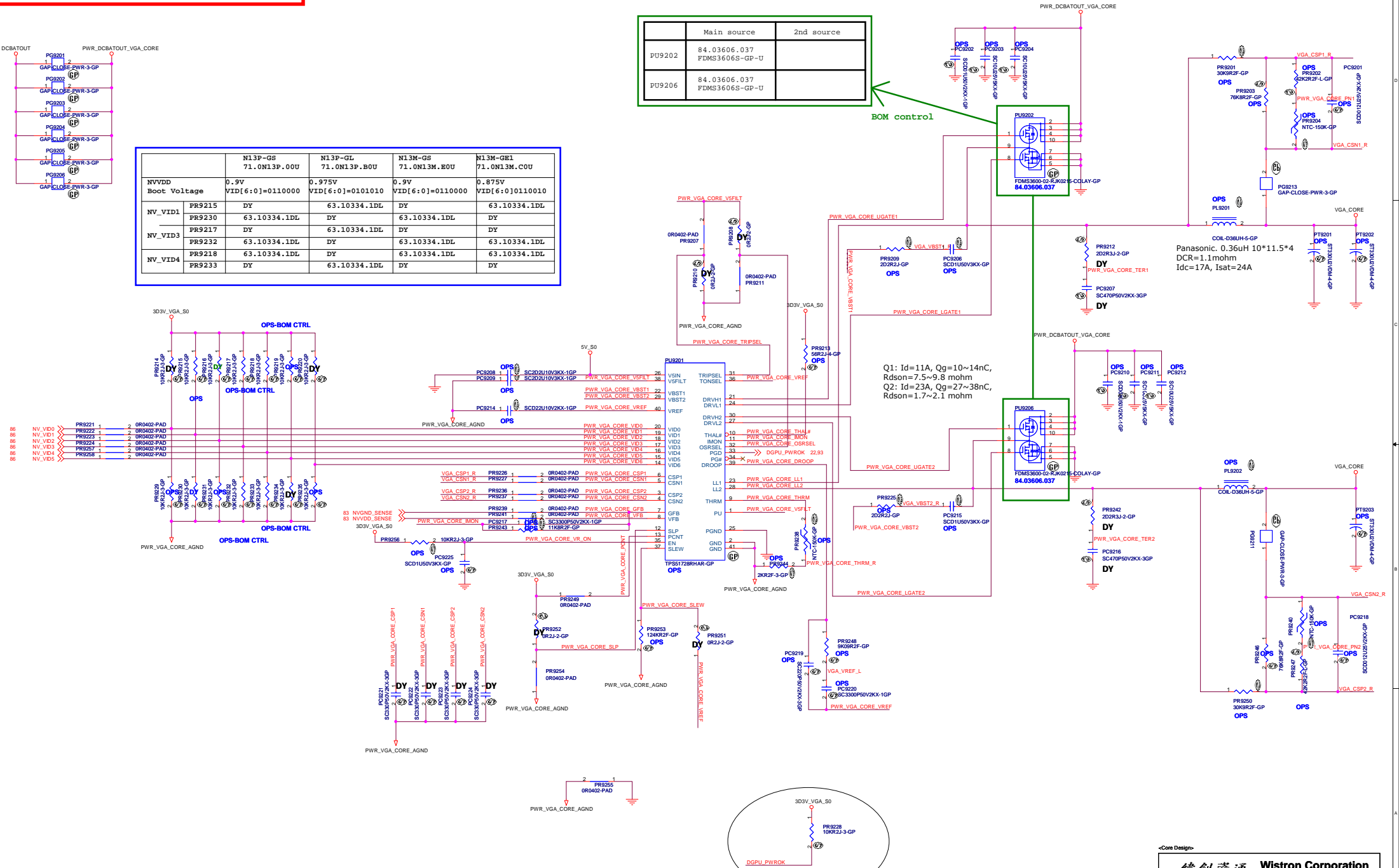
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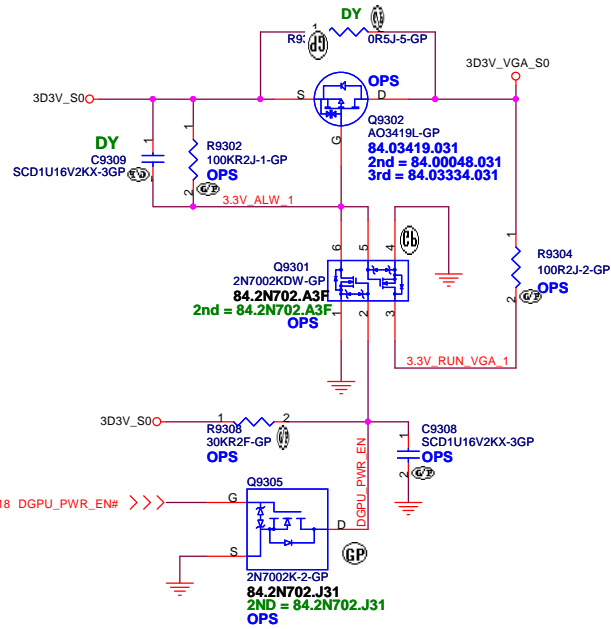
Title **CHANNEL-C_VRAM7,8 (4/4)**

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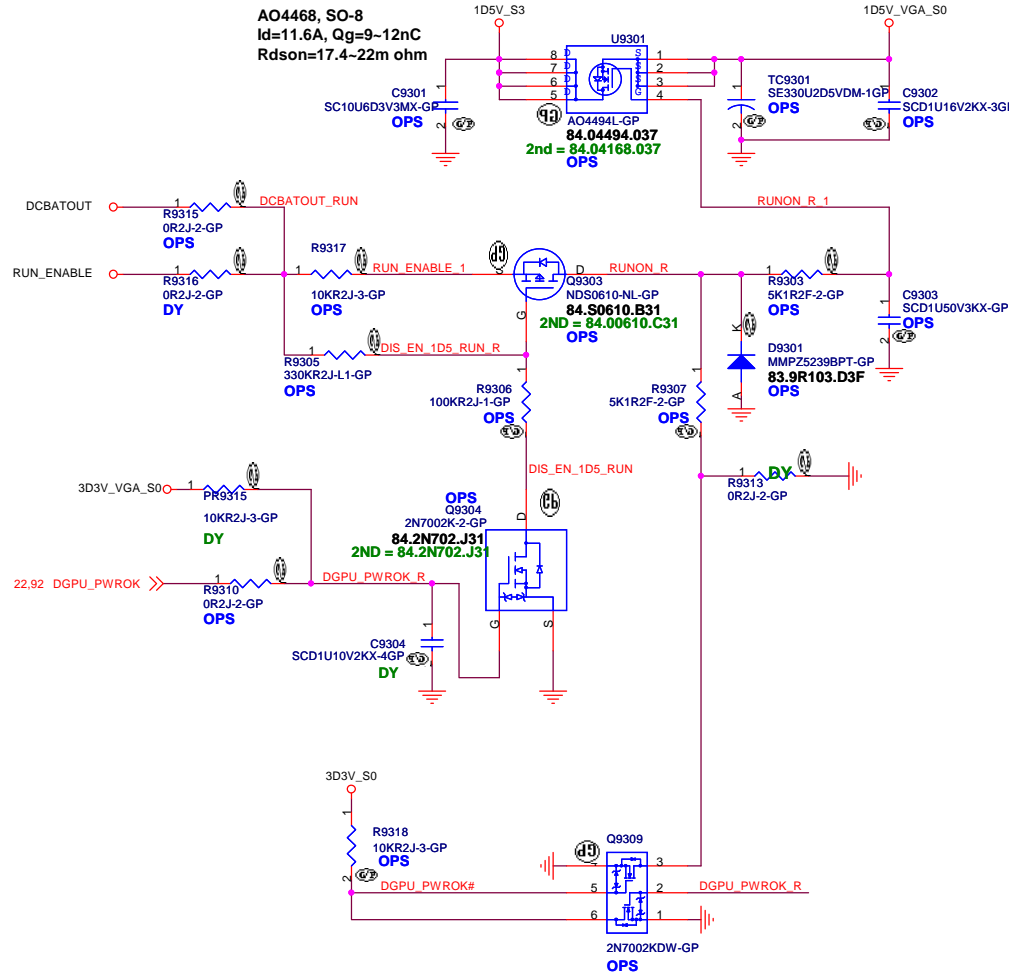
SSID = PWR.Plane.Regulator_GFX



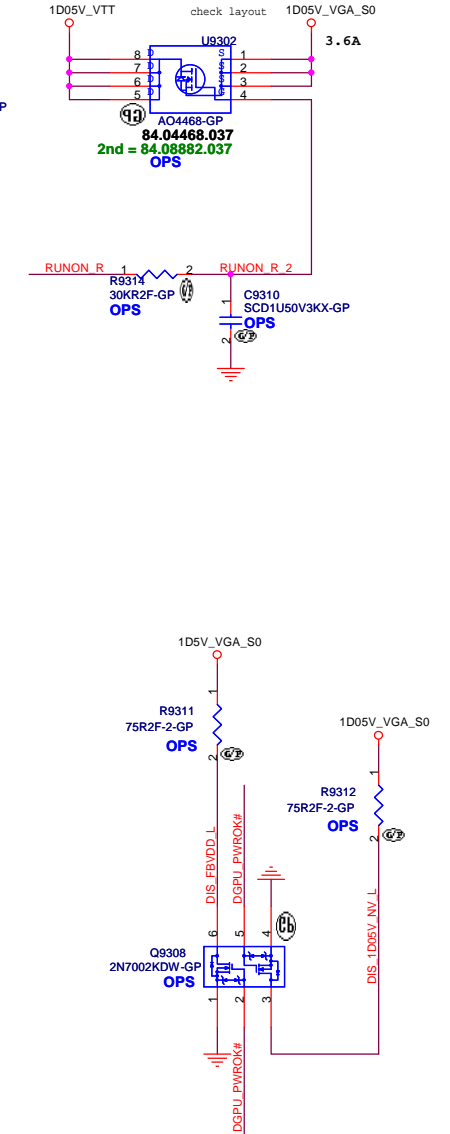
+3VS to 3.3V_DELAY Transfer



1D5V_VGA_S0



1.05V to 1.05V_VGA_S0 Transfer



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Title DISCRETE VGA POWER

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D

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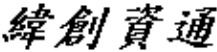
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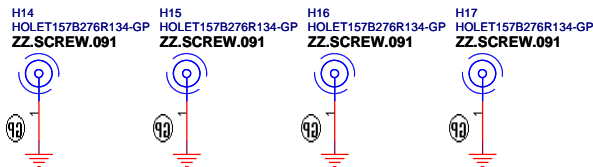
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Title Reserved			
Size A4	Document Number LA480		Rev SD
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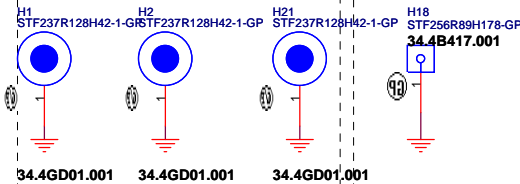
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Title TOUCH PANEL			
Size A4	Document Number LA480		Rev SD
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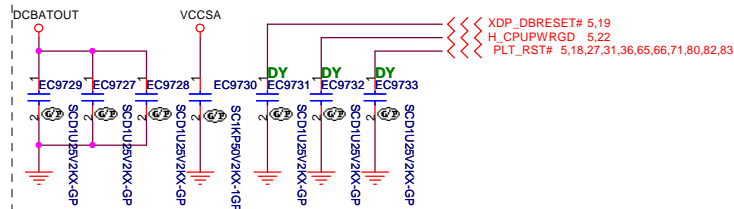
CPU Plate



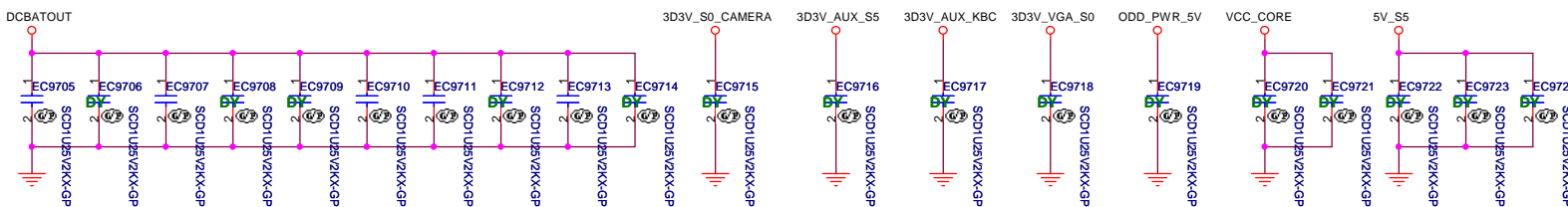
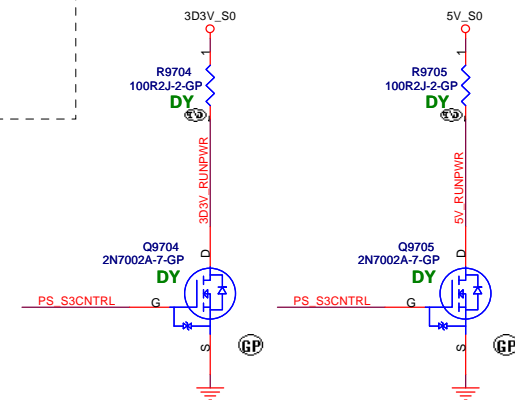
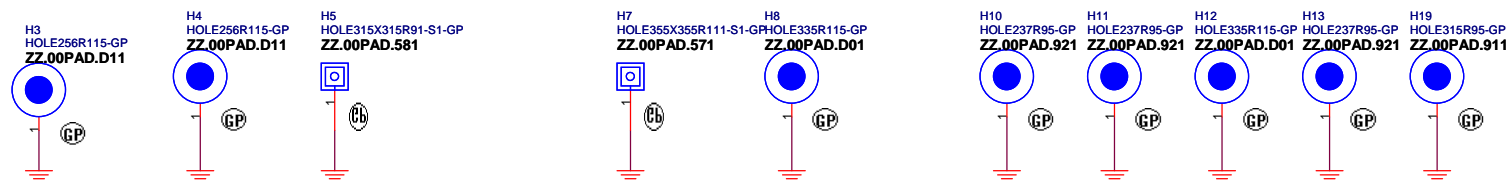
VGA Std-Off



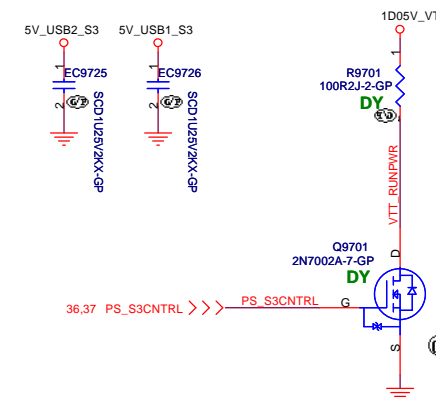
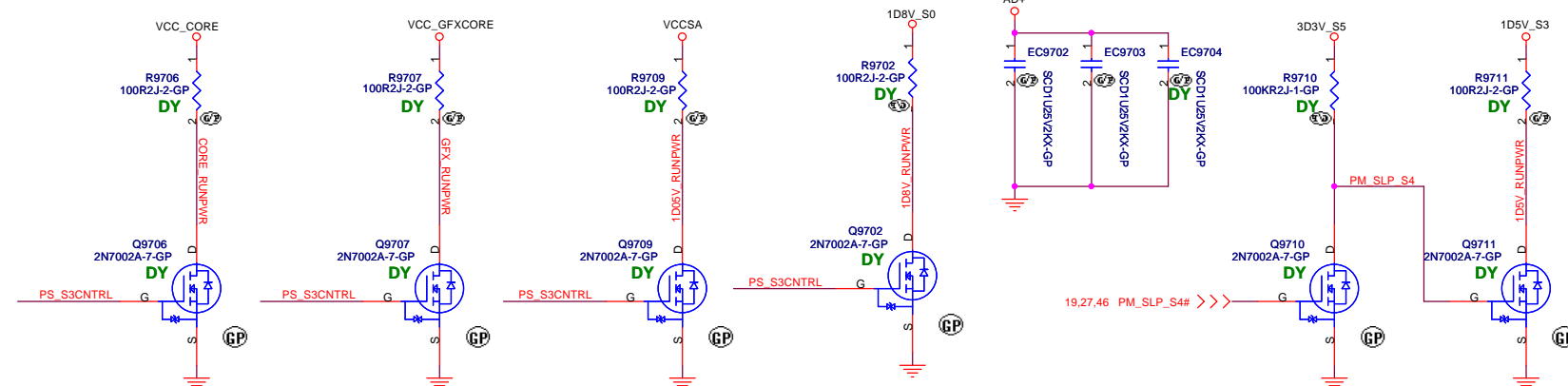
MINI PCIE



14" Structure boss



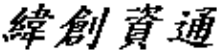
For Discharge



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Title	UNUSED PARTS/EMI Capacitors	
Size	Document Number	Rev
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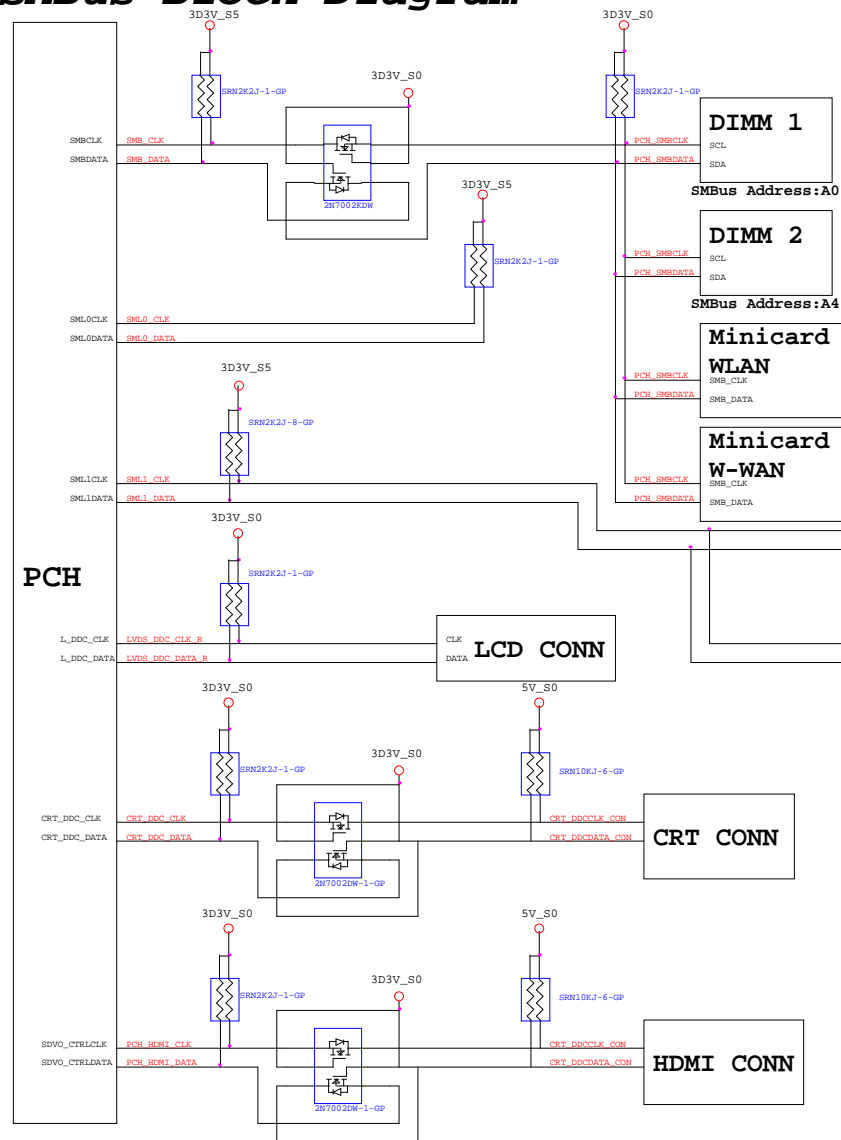
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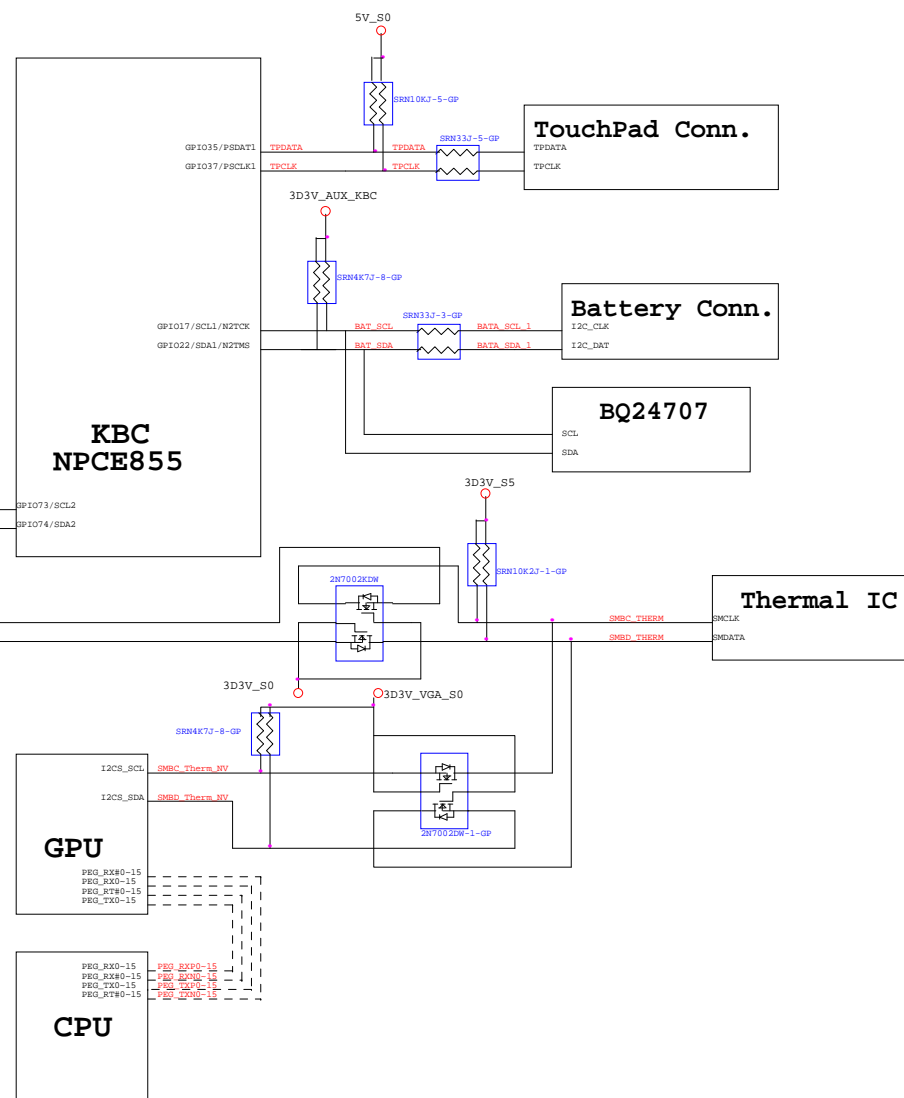
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Title			
Change History			
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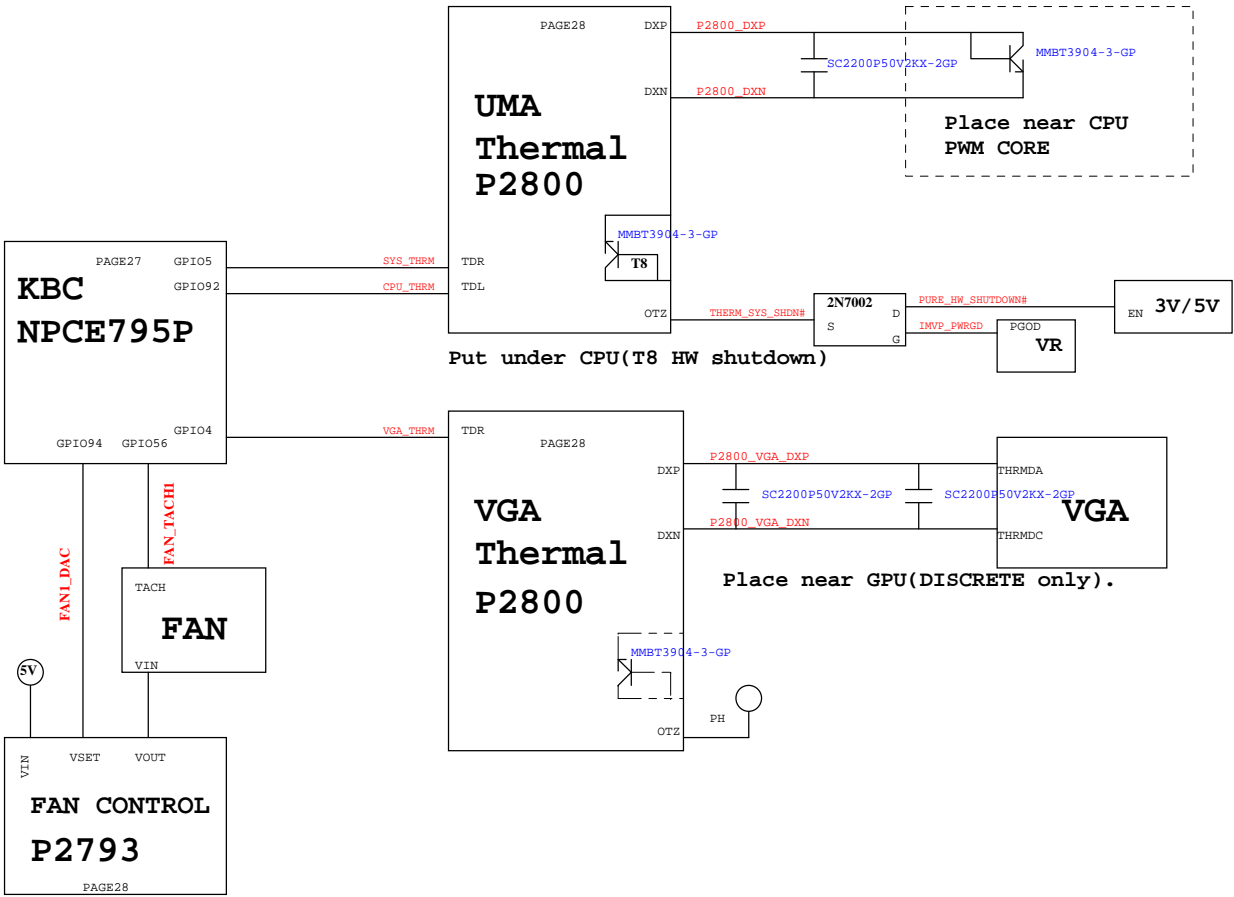
PCH SMBus Block Diagram



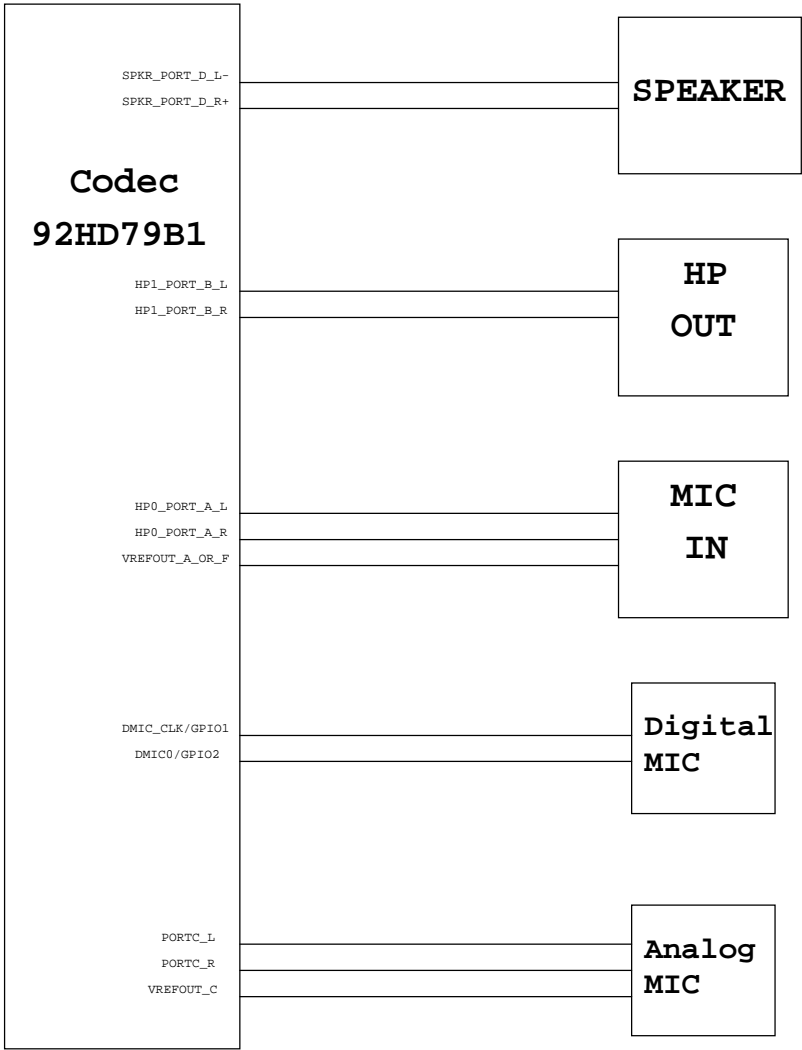
KBC SMBus Block Diagram



Thermal Block Diagram



Audio Block Diagram



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